Doctoral Dissertation

Shibaura Institute of Technology

Fabrication of multilayer graphene by solid-phase reaction and application to gallium nitride based Schottky diodes

September, 2017

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FABRICATION OF MULTILAYER GRAPHENE BY SOLID-PHASE REACTION AND APPLICATION TO GALLIUM NITRIDE BASED SCHOTTKY DIODES

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A thesis submitted in fulfilment of the

requirements for the award of the degree of

Doctor of Engineering

Shibaura Institute of Technology

CANDIDATE'S DECLARATION

It is hereby declared that this thesis or any part of it has not been submitted elsewhere for the award of any degree or diploma.

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Dedicated

To

My beloved parents and my honorable supervisor

Acknowledgements

I am extremely delighted to express my indebtedness and deepest sense of gratitude to my honorable supervisor ***Dr. Kazuyoshi Ueno,*** *Professor, Department of Electronic Engineering, Shibaura Institute of Technology (SIT), Japan, for his supervision, comprehensive support, and valuable suggestions that inspired and accelerate me to complete this research work. This dissertation would never being possible without his cordial support and directions.*

I express my deepest sense of gratitude and profound respect to my supervisor in sub-charge, ***Dr. Hiroyasu Ishikawa,*** *Professor, Department of Electronic Engineering, Shibaura Institute of Technology (SIT), Japan, for fruitful discussions about some topics related to my research.*

I am grateful to ***Prof. Kan Akatsu*** *(SIT),* ***Prof. Shinichi Tanaka*** *(SIT), and* ***Prof. Eiichi Kondoh*** *(University of Yamanashi) for their kind agreement in reviewing my dissertation.*

Very special thanks to Shibaura Institute of Technology for giving me opportunity to carry out doctoral program. I feel to thank ***Mikiko Nikami*** *for her cordial support and help during my stay at SIT. I would like to thank all the members of Nano-electronic Laboratory, SIT for their support and help in the laboratory as well as outside. Working with them during these past years has truly been a delight.*

I would like to offer a very very special thanks to ***Research Center for Green Innovation (RCGI)****, SIT, for financial support by providing me a special scholarship. I also grateful to all the members of* ***Research Center for Power Electronics,*** *SIT.*

I would like to express my gratitude to my parents, my beloved wife ***Mrs. Sharmin Akter****, and my son* ***Tawhid Sahab*** *for their inspiration and support during this work.*

Abstract

Now a days, global warming becomes one of the most focusing issue for the scientists and engineers all over the world. Global warming caused mainly due to the emission of greenhouse gases. A major part of energy used worldwide comes from fossil fuel combustion. To convert the fossil fuels to usable energy form greenhouse gas emissions are occurring and natural processes can absorb some of this emitted greenhouse gases while the rest of the emitted greenhouse gases are mainly responsible for the global warming. Therefore, to reduce the emission of greenhouse gases it is needed to reduce the energy consumption in society as well as industries to deduce the technological impact on greenhouse gas emission. For industrial aspect it is needed to fabricate high energy efficient and highly reliable devices to make the device environment friendly. The device fabrication temperatures should be reduced to decrease the energy consumption. Wide band-gap gallium nitride (GaN) and related materials are chemically stable compound semiconductors, and have attracted considerable interest for application in opto-electronic device and high power/high temperature electronic device. Devices made of nitride-based materials include metal-semiconductor-metal (MSM) ultraviolet (UV) light photo-detectors, metal semiconductor field-effect transistors (MESFETs), high electron mobility transistors (HEMTs), metal-oxide semiconductor field-effect transistors (MOSFETs), heterojunction bipolar transistors (HBTs) and Schottky rectifier diodes. For these applications, high quality Schottky contacts have been key factors in improving performance, reliability, and thermal stability.

Graphene/multilayer graphene (MLG) are being extensively studied for various applications such as narrow interconnects, an active or passive layer in electronic and optoelectronic semiconductor device and many more for its outstanding physical, electrical, optical, and mechanical properties and expected high thermal stability due to its high melting point. For the application of MLG as an interconnect material, improvement of crystallinity and uniformity at comparatively lower temperature is still a challenge. For the application of MLG to semiconductor devices (such as GaN power devices), transfer-free deposition is better than those requires an additional transfer process. Several research groups reported on transfer-free deposition of MLG on n-GaN by thermal CVD. But, the deposition temperature is as high as 950 ^{o}C and the MLG crystallinity is not good. Therefore, transfer-free deposition of MLG on n-GaN substrate with improved crystallinity and lowering the deposition temperature is required for most of the promising applications of MLG based n-GaN devices. This dissertation

is concerned with the fabrication of MLG on SiO_2 and n-GaN substrates by solid-phase reaction (SPR) and application especially on n-GaN based Schottky diodes. MLG deposition by SPR has an advantage of transfer-free deposition on desired substrate. The improvement of crystallinity and uniformity are another challenge of our present work.

To improve the crystallinity of MLG on SiO_2 by SPR, a new approach of application of current stress during annealing of sputtered carbon doped cobalt (Co-C) layer was proposed. The Co layer acts as a catalyst for the SPR to occur. The effects of current stress on the formation and crystallinity of MLG films were investigated by comparing the characteristics of the films annealed at the same temperature with and without current by taking into account the temperature rise due to Joule heating. The characteristics obtained by Raman spectroscopy, scanning electron microscopy (SEM), transmission electron microscopy (TEM), and X-ray diffraction (XRD) measurements revealed that the MLG films produced were crystalline in nature and their crystallinity increased with applied current stress at the same temperature. From SEM observations, beside Joule heating, reduction of nucleation sites of MLG induced by current stress may be the potential reason for the improvement of the crystallinity of MLG films. However, the MLG growth was not uniform over the entire substrate as was confirmed by SEM images. From the cross-sectional TEM image, it was found that the MLG growth took place at the sides of the Co. The non-uniform growth of MLG might be due to the growth originates from the crystalline facets. From the XRD measurements, Owing to the formation of new fcc phases of Co after applying current stress at the same temperature, it is easier for carbon atoms to form MLG at the fcc step site. Therefore, the predominance of fcc Co after applying current stress may be another reason for the improvement of MLG crystallinity. The uniformity of MLG films were improved by depositing an additional Cu capping layer over the Co-C layer. When a Cu capping layer is deposited over the Co-C layer, the Cu layer can suppress the agglomeration of Co, which leads to the uniform precipitation of MLG, since Cu does not form an alloy with Co at the annealing temperature used in our experiment.

The second approach of our present research was transfer-free deposition of MLG on n-GaN by SPR without extra catalyst by annealing sputtered a-C on n-GaN. Diamond like carbon films were found to form by annealing the a-C layer on n-GaN at temperatures between 800 and 1000 ^{o}C. The surface uniformity of the samples were seen to be improved with the increase of annealing temperature. Crystallization of a-C occurred due to high temperature annealing or self catalization of Ga by breaking of GaN into Ga and N_2 at high temperature as was confirmed by XRD measurement. However, by this method the nanocarbon crystallinity was poor and the fabrication temperature was as high as 1000 ^{o}C. For the reflection of

performance of an MLG based device improvement of crystallinity of nano-carbon film similar to MLG are required. The lowering of the deposition temperature are required to reduce C diffusion to GaN.

To improve the crystallinity and uniformity of the MLG films on n-GaN by SPR an extra Co layer as catalyst was involved for SPR to occur. At first, MLG was deposited by annealing room temperature (RT)-sputtered Co/C layer on n-GaN. The characterization made by Raman spectroscopy, it was found that the graphitization stopped after annealing the structure at 750 °C. From the XRD measurement of RT sputtered and annealed Co/C layer, it was found that the reaction between Co and GaN took place and a Co_2O_3 phase appeared after annealing at 750 °C, that might be responsible for non-graphitization. Also from the SEM images of the RT-sputtered and annealed film, it was found that the surface of the MLG films were not uniform over the entire substrate. The non-uniformity was considered due to the difference in thermal expansion between GaN and the sputtered films. The MLG crystallinity and uniformity were improved significantly after applying heat sputtering for the deposition of amorphous C and Co layers in comparison that with conventional RT sputtering. The growth conditions for MLG with improved crystallinity and uniformity were optimized as follows: 150 ^{o}C sputtering of the Co/C layers annealed at 650 ^{o}C. Decreasing the difference in the thermal expansion between GaN and Co/C, the suppression of the reaction between GaN and Co, and by cleaning of the GaN surface before sputtering might be the reasons for the improvement in the crystallinity and uniformity. This method of MLG fabrication will be promised with further success in fabricating an MLG based GaN device. Our next approach was to fabricate a device with MLG deposited by our proposed method.

The fabrication of an MLG based device with transfer-free deposition of MLG on n-GaN by SPR has been demonstrated by our proposed method. The MLG/n-GaN Schottky barrier diodes (SBD) were fabricated with transfer-free deposition of MLG on n-GaN by SPR. The as-deposited MLG/n-GaN diode showed rectification with a barrier height of 0.72 eV. For the as-deposited diodes, Schottky barrier height (SBH) was found to be in good agreement with other available reported values. The thermal stability of the diodes were measured by measuring the I-V characteristics after annealing the diodes without annealing and after annealed at various temperatures ranging from 200 to 500 °C in vacuum of 5×10^{-3} Pa and was compared with a conventional Ni/n-GaN diode. It was found that the MLG/n-GaN diodes showed better thermal stability with more stable SBH than a conventional Ni/n-GaN diode annealing up to 500 °C. The diode properties calculated by TE model and Cheung's method was found to be in good agreement with one another. The unaffected interface reaction with

annealing and the prevention of Au diffusion to n-GaN due to action of MLG as Au diffusion barrier layer was confirmed by XRD measurement is considered to be the reason behind the thermal stability. However, the series resistance of MLG/n-GaN diode was found to be higher than the Ni/n-GaN diode. Reduction of series resistance will be necessary for promising application of our MLG/n-GaN SBD with MLG deposited by our proposed method.

To reduce the series resistance of fabricated MLG/n-GaN diode, the top contact metal was changed from Au to Cu, since, the resistivity of Cu is lower than Au. Upon changing the top metal, there was no significant reduction in series resistance, therefore, the series resistance of our fabricated device is predominated by MLG layer. Our next approach is to decrease the MLG thickness as small as possible. This work is currently underway.

Finally, achievements of this dissertation are as follows: 1) Improvement of MLG crystallinity on dielectric substrate at comparatively lower temperature by SPR, 2) Uniform deposition of MLG on SiO_2 substrate with additional Cu layer as capping on Co-C layer, 3) Transfer-free deposition of MLG on n-GaN for the first time by SPR with improved crystallinity and uniformity at comparatively lower temperature, 4) Fabrication of an MLG/n-GaN Schottky barrier diode with higher thermal stability than a Ni/n-GaN Schottky diode with transfer-free deposition of MLG by our new method. With further improvement, our method will be promising for low resistance interconnect and improved thermal stability of n-GaN Schottky diodes.

The implementation of our new proposed method of MLG fabrication on SiO_2 substrate will lead to fabricate a low resistance narrow interconnect. MLG fabrication on n-GaN by our proposed method will lead to fabricate a wide-band gap semiconductor power device (n-GaN) with thermally stable Schottky contact that can be driven at high frequency and high temperature, and downsizing of the device. By replacing conventional Si power device with GaN power device, energy saving is anticipated. The fabrication temperature is lowered that will also reduce the energy consumption from the conventional energy sources during fabrication and will reduce the emission of greenhouse gases responsible for global warming.

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International Journal

1. M. S. Uddin, H. Ichikawa, S. Sano and K. Ueno, "Improvement of multilayer graphene crystallinity by solid-phase precipitation with current stress application during annealing", Japanese Journal of Applied Physics **55**, 06JH02 (2016).

2. M. S. Uddin and K. Ueno, "Fabrication of a Schottky diode with transfer-free deposition of multilayer graphene on n-GaN by solid-phase reaction", Japanese Journal of Applied Physics, **56**, 04CP08 (2017).

3. M. S. Uddin and K. Ueno, "Thermal stability of a Schottky diode fabricated with transfer-free deposition of multilayer graphene on n-GaN by solid-phase reaction", Japanese Journal of Applied Physics, **56**, 07KD05 (2017).

International Conferences

1. M. S. Uddin, H. Ichikawa, S. Sano and K. Ueno, "Improvement of multilayer graphene crystallinity by solid-phase precipitation applying current stress during annealing", ADMETA plus 2015, no 7-4, pp 194-195. Oral presentation.

2. M. S. Uddin and K. Ueno, "Fabrication of a Schottky diode with direct deposition of multilayer graphene on n-GaN by solid phase reaction", SSDM 2016, no K-4-04, pp 495-496. Oral presentation.

3. M. S. Uddin and K. Ueno, "A noble Schottky diode involving direct deposition of multilayer graphene on n-GaN by solid-phase reaction", ADMETA plus 2016, no. 7-3, pp 94-95. Oral presentation.

Domestic conferences

1. M. S. Uddin, H. Ichikawa, S. Sano and K. Ueno, "Fabrication of multilayer graphene by solid phase precipitation with current stress", SDM 2016 no 187 [ISBN: 978-4-86348-534-1], pp. 30-33. Oral presentation.

2. M. S. Uddin, H. Ichikawa, S. Sano and K. Ueno, "Effect of current stress on formation and crystallinity of multilayer graphene by solid phase precipitation", 10th SEATUC Symposium 22nd – 24th February 2016 [ISSN 1882-5796], no OS11-2, p.148. Oral presentation.

3. M. S. Uddin and K. Ueno, "Catalyst free direct deposition of multilayer graphene on GaN by solid phase precipitation" presented at the 63rd JSAP spring meeting 2016, no. 20P-P9-5. Poster presentation.

4. M. S. Uddin and Kazuyoshi Ueno, “Improvement of multilayer graphene (MLG) / n-GaN Schottky diode properties fabricated with transfer-free deposition of MLG on n-GaN by solid-phase reaction” presented at the 81th Symposium on Semiconductors and Integrated Circuits Technology 2017, no P4. Poster presentation.

Awards

1. Silver poster award in 4th Green Innovation Symposium held at Shibaura Institute of Technology in February 22, 2017.
2. Poster award in 81th Symposium on Semiconductors and Integrated Circuits Technology 2017, held at Tokyo University of Science on August 25-26, 2017.

CHAPTER ONE
INTRODUCTION

1.1. Overview

The 21st century has been termed the Century of the Environment [1]. With growing world population; intensification of agricultural and industrial activities; contamination of air, soils and aquatic ecosystems; global warming; and global climate change; environmental issues are becoming a major focus of engineering and scientific attention [1]. Fossil fuels — coal, petroleum, and natural gas — are our main sources of energy, producing the vast majority of fuel, electricity, and heat used by people across the globe. In 2005 a whopping 86 percent of energy used worldwide came from fossil fuel combustion, and right now the number isn't much lower at about 85 percent. Unfortunately fossil fuels are also the primary culprit behind climate change. To convert the fossil fuels to usable energy form greenhouse gas emissions are occurring and natural processes can absorb some of this emitted greenhouse gases while the rest of the emitted greenhouse gases are mainly responsible for the global warming. Therefore, to reduce the emission of greenhouse gases it is needed to reduce the energy consumption in society as well as industries to deduce the technological impact on greenhouse gas emission. For industrial aspect it is needed to fabricate high energy efficient and highly reliable devices to make the device environment friendly. The device fabrication temperatures should be reduced to decrease the energy consumption.

Nanomaterials possess unique properties, owing to their nanoscale dimensions, that can be used to design novel technologies or improve the performance of existing processes. Nanomaterials have found multiple applications in energy production, fabrication of high efficient device, and contaminant sensing, and a growing amount of literature describes how novel nanomaterials may be used to address major environmental challenges [2-6]. The latest material to capture the attention of researchers is graphene, a two-dimensional layer of carbon atoms arranged in a hexagonal crystalline structure [7]. The interest in graphene originates from its unique physicochemical properties, notably the lower resistivity [8,9], high thermal conductivity [10,11], high current capacity [12,13], and mechanical strength.

1.2. Background and objectives

Owing to the global warming issue mentioned in the previous section, it is needed to find low power consumption device such as low resistance interconnect. The most commonly used

interconnect material is copper. Emission of greenhouse gases can be reduced also by fabricating a high-efficiency semiconductor power device that can be operated at high frequency and high temperature. Wide band-gap gallium nitride (GaN) and related materials are chemically stable compound semiconductors, and have attracted considerable interest for applications in opto-electronic devices and high power/high temperature electronic devices. Devices made of nitride-based materials include metal-semiconductor-metal (MSM) ultraviolet (UV) light photo-detectors, metal semiconductor field-effect transistors (MESFETs), high electron mobility transistors (HEMTs), metal-oxide semiconductor field-effect transistors (MOSFETs), heterojunction bipolar transistors (HBTs) and Schottky rectifier diodes. For these applications, high quality Schottky contacts have been key factors in improving performance and reliability. The thermally stable and reliable Schottky contact is essential for the application of electronic and optoelectronic devices. To improve the performance of above mentioned devices, it is needed to find an interconnect material as well as a highly reliable and thermally stable Schottky contact material. Graphene/multilayer graphene (MLG) can be used as an alternate interconnect material or Schottky contact metal due to its outstanding physical, electrical and optical properties.

Copper has been used as an interconnect material since the 200 nm node of ultralarge-scale integrated (ULSI) circuit was developed. However, resistance increase and reliability degradation are becoming problems owing to the shrinkage of the interconnect size [14-16]. Multilayer graphene (MLG) is considered to be the new candidate material for narrow interconnects owing to its potentially lower resistivity [17,18], higher thermal conductivity [19,20], and higher current carrying capacity [21,22] than Cu. One of the challenges for the MLG interconnect fabrication is the growth process for MLG with high crystallinity with improved uniformity at a lower temperature, because the high crystallinity is essential to obtain a low resistance with less scattering and a low temperature such as that blow 700 °C is required for the interconnect process. Another challenge of MLG fabrication for interconnect application is the transfer-free deposition. For MLG deposition by chemical vapor deposition, it requires an extra transfer step of graphene or MLG from one substrate to another. To avoid this, transfer-free deposition of MLG is more promising for interconnect applications.

Graphene/MLG are being studied extensively for the fabrication of GaN based power devices. Graphene or MLG is expected as an alternative Schottky metal on n-GaN owing to its outstanding physical and optical characteristics such as high intrinsic electron mobility, quantum electronic transport, low optical absorption, and good chemical and mechanical stabilities [23-28], and its high barrier height, low reverse leakage current, and high thermal

stability have been reported [29,30]. Graphene has been synthesized by various methods, among which chemical vapor deposition (CVD) on a metal substrate is the most common method for obtaining large-area high-quality graphene films. However, for most of the device fabrication methods, graphene synthesized on a metal substrate requires an additional transfer step [29,30], which may not be ideal for many applications. Several research groups reported on the direct deposition of MLG on n-GaN by thermal CVD [31,32]. However, the MLG fabrication temperature was as high as 950 ^{o}C and the MLG crystallinity was not good enough (D peak intensity were greater than G peak intensity). In this context, synthesis of transfer-free graphene/MLG directly on n-GaN with higher crystallinity than the reported one mentioned in Ref. 31,32, can be a promising approach for obtaining the most interesting physical and electrical properties of graphene/MLG for device applications. Another issue of MLG fabrication on n-GaN is the high deposition temperature. Lowering of the MLG deposition temperature is required to reduce the C diffusion through n-GaN and lowering the energy consumption during fabrication.

The purpose of our present study is transfer-free deposition of MLG on dielectric substrate (SiO_2) and semiconducting substrate (n-GaN). We ought to improve the MLG crystallinity and uniformity deposited on SiO_2 and n-GaN substrate for potential application as interconnect and power device fabrication. The lowering of the fabrication temperature is another challenge of the present study. Finally, our main target is to fabricate an MLG/n-GaN SBD with transfer-free deposition of MLG on n-GaN at comparatively lower temperature. We ought to measure the thermal stability of the fabricated diode and compare it with a conventional SBD.

1.3. Graphene: its discovery, properties, fabrication methods and applications

1.3.1 Graphene and its discovery

Graphene is the newest member of the family of carbon allotropes. The study of carbon allotropes is always in important issue in the field of applied material science and engineering. The possible allotropes of carbon is shown in Fig. 1.1.

The term graphene is not very new research topic. The theoretical prediction of graphene was found more than fifty years ago [33]. However, it took quite long for scientist to make a 2-D material in 3-D nature. Graphene's odd dimensionality brings excellent properties and novel applications.

Probably graphene stands as the top of all the carbon forms, or at least as the last member in the carbon family. Graphene consists of a single layer of carbon atoms densely packed in a hexagonal lattice (2500 billion at/cm^2) that means it is a single layer of graphite. Its bounds are sp^2 hybridized, what forms three strong in plane σ bonds per carbon atom. The interatomic distance between this strong bonds are 0.142 nm, the shorter distance of all the materials that is responsible for outstanding mechanical properties of graphene. Out of graphene plane, the not completely filled pz orbitals (also called π orbitals) forms weak π bonds and are the responsible of the conductive properties. This honeycomb structure is the basis of other allotropes of carbon such as graphite, carbon nanotubes and fullerenes (Fig. 1.2).

In the early 20th century, Landau and Peierls argued that strictly 2D crystals were thermodynamically unstable and could not exist [34, 35]. In 1947, their theory pointed out that thermal fluctuation in low-dimensional crystal lattices should lead to displacements of atoms comparable to interatomic distances at any finite temperature [36]. The argument was extended thickness as its surface/volume ratio is increased due to the fact that a material melting begins in its surface [34,37]; and the films become unstable (segregate into islands or decompose) by Mermin 30 years later [35] and was strongly supported by a large number of experimental observations. Indeed, the melting temperature of thin films rapidly decreases with decreasing thickness asits surface/volume ratio is increased due to the fact that a materialmelting begins

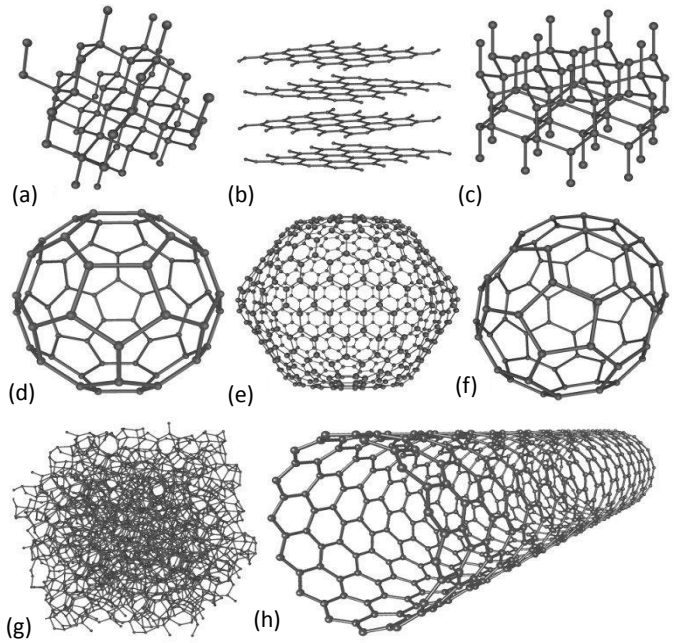

Figure 1.1. The structures of eight allotropes of carbon: (a) Diamond, (b) Graphite, (c) Lonsdaleite, (d) C_{60} (Buckminsterfullerene), (e) C_{540} Fullerene, (f) C_{70} Fullerene, (g) Amorphous carbon, and (h) Single-walled carbon nanotube, image [38].

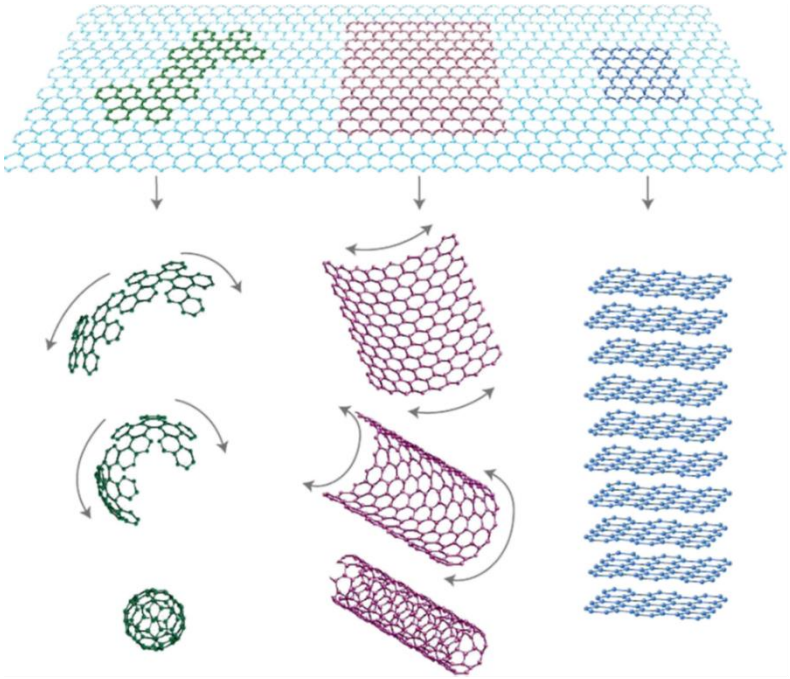

Figure 1.2. Mother of all graphitic forms. Graphene is a 2D building material for carbon materials of all other dimensionalities. It can be wrapped up into 0D buckyballs, rolled into 1D nanotubes or stacked into 3D graphite. These approximations (0D, 1D, and 2D) are due to the reduced dimensions of the nanostructures, image [34].

in its surface; and the films become unstable (segregate into islands or decompose) at a thickness of, typically, dozens of atomic layers [39,40]. Also the latent heats show large size-dependent fluctuations. In some cases, the melting temperatures change by hundreds of degrees with the addition of a single atom [41]. For this reason, atomic monolayers have so far been known only as an integral part of larger 3D crystal, usually grown epitaxially on top of monocrystals with matching crystal lattices. Without such a 3D base, 2D materials were presumed not to exist. Yet in 1962, the word "graphene" started to be used in order to define a graphite monolayer.

The experimental discovery of graphene [42] in 2004 and other free-standing 2D atomic crystals [43-45] showed the world that this kind of material can physically exist. This made a movement in graphene research. Two scientists from the University of Manchester (United Kingdom), Andre Geim and Konstantin Novoselov (Fig. 1.3), isolated for the first time a layer of graphene using ordinary scotch tape and graphite. This particular method, known as mechanical exfoliation, leaded to the acknowledgment in 2010 with the Nobel Prize in Physics for the discovery of graphene and its characterization. The authors prepared graphitic sheets of thicknesses down to a few atomic layers and fabricated devices from them and studied their

electronic properties [41]. Using a few layer graphene and new monolayer graphene they succeeded in fabricating a metallic FET in which conducting channel was able to be switched between 2D electrons and hole gases by changing the gate voltage.

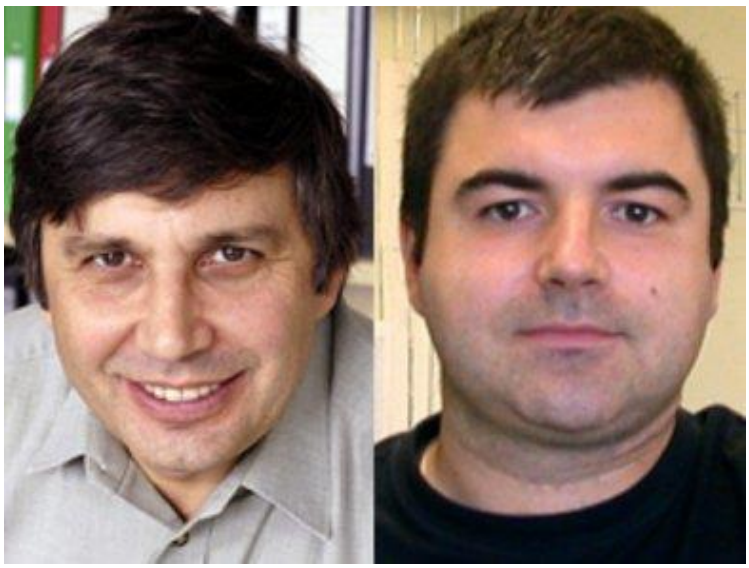

Figure 1.3. Andre Geim and Konstantin Novoselov, University of Manchester, UK, image [34].

1.3.2. Graphene properties

Graphene is considered as a two-dimensional sheet of sp^2 bonded carbon atoms arranged in a honeycomb crystal structure with two carbon atoms in each unit cell. Graphene's lattice structure can be considered as two equivalent triangular sublattices A and B with inversion symmetry (Fig. 1.4(a)). The corresponding energy bands of these two sublattices intersect at zero energy at K points, called Dirac points, of reciprocal lattice [Fig. 1.4(b) and 1.4(c)]. The dispersion relation near Dirac points is linear, and has no band gap. Thus, graphene is considered as a zero band gap semiconductor or a semimetal in which Dirac Equation governs the charge carrier behavior near Dirac points at low energies [46].

Graphene's linear dispersion relation at low energies near the six Dirac points can be described by equation (1.1), leading to zero effective mass for electrons and holes which move with a constant speed called Fermi velocity.

$$E = \pm \frac{h}{2\pi} \vartheta_f \sqrt{k_x^2 + {k_y}^2} \qquad (1.1)$$

Where ϑ_f is the Fermi velocity of electron and holes in graphene [48]. So, considering linear dispersion relation in graphene, charge carriers are regarded as Massless Dirac Fermions in analogy to relativistic massless particles like phonons [49, 50].

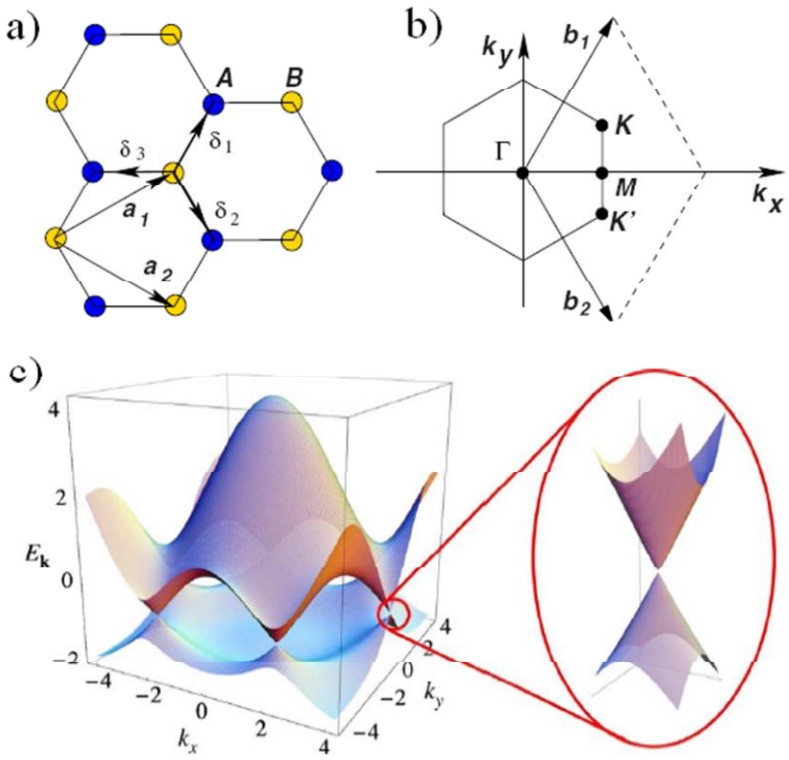

Figure 1.4. a) Lattice structure of graphene consists of two trigonal lattices A and B. b) First Brillouin zone of graphene lattice. c) Dispersion relation of graphene in fist Brillouin zone, image [47]

The outstanding electronic properties of graphene are at the center of attention of scientists and engineers all over the world from its discovery. Charge carriers of graphene exhibit ballistic transport along submicron length [47]. Also, the reported value of carrier mobility is high and is 15000 $cm^2/V.s$ for graphene on SiO_2 substrate [49], 27000 $cm^2/V.s$ for epitaxial graphene [50] and 200000 $cm^2/V.s$ for suspended graphene [51, 52]. However, the carrier mobility of graphene based electronic devices is limited due to different scattering mechanisms, especially from charged impurity centers [53].

Graphene possesses another stand-out properties is its inherent strength. Due to the strength of its 0.142 Nm-long carbon bonds, graphene is considered as the strongest material ever discovered, with an ultimate tensile strength of 130,000,000,000 Pascals (or 130 gigapascals), compared to 400,000,000 for A36 structural steel, or 375,700,000 for Aramid (Kevlar). Not only is graphene extraordinarily strong, it is also very light at 0.77milligrams per square metre (for comparison purposes, 1 square metre of paper is roughly 1000 times heavier). It is often said that a single sheet of graphene (being only 1 atom thick), sufficient in size enough to cover a whole football field, would weigh under 1 single gram.

Graphene's ability to absorb a rather large 2.3% of white light is also a unique and interesting property, especially considering that it is only 1 atom thick. This is due to its aforementioned electronic properties; the electrons acting like massless charge carriers with very high mobility. A few years ago, it was proved that the amount of white light absorbed is based on the Fine Structure Constant, rather than being dictated by material specifics. Adding another layer of graphene increases the amount of white light absorbed by approximately the same value (2.3%). Graphene's opacity of $\pi\alpha \approx 2.3\%$ equates to a universal dynamic conductivity value of $G=e2/4\hbar$ (±2-3%) over the visible frequency range.

The experimentally observed other exceptional properties of graphene are its high thermal conductivity at RT, high melting point, chemically inertness, high transparency, and mechanical stability.

1.3.3. Different methods of graphene/MLG fabrication

Since the discovery of graphene through mechanical exfoliation of pyrolytic graphite, several approaches from many disciplines have been developed in order to obtain it. However, different synthesis methods lead to "different qualities and characteristics" of the graphene produced. In this section, we will briefly describe some commonly used techniques for the fabrication of graphene or multilayer graphene (MLG).

1.3.3.1. Mechanical exfoliation

Mechanical exfoliation by cleaving bulk layered material is the most straightforward method to obtain a monolayer 2-D material. By applying a sufficient force perpendicular to the plane directions, such that the weak Van der Waals forces between sheets can be overcome, and then repeating this process over and over again, eventually a single atomic layer can be isolated and placed onto a substrate for characterization. Novoselov et al. used an adhesive tape to peel off graphene layers [41] as has been described in the previous chapter. They first prepared square HOPG with 20 mm to 2 mm in length and then attached them to photoresist. Using the adhesive tape, graphite sheets were peeled off from the photoresist, still leaving mono- to few-layered graphene. These layers were finally brought onto a Si substrate by releasing the photoresist from the tape by an acetone treatment. Different steps of graphene/MLG fabrication by this method is shown in Fig. 1.5. Firstly, (a) the adhesive tape is pressed onto the HOPG. In second step, (b) the tape is pilled of when some layers sticked on the surface. Thirdly, (c) the tape is pressed onto the surface of the target substrate. Finally, (d) the tape is peeled off when the layer stick to the target surface.

The advantages of this method are as following

- Safe and simple process
- Few layer graphene can be easily obtained
- The chances of impurity in the graphene/MLG so obtained are less
- Sample preparation is simplified

The disadvantages of this method can be summarized as follows

- Large area MLG formation is a challenge
- Reliability of obtaining similar structure is low
- Layer number is not uniform throughout the area.

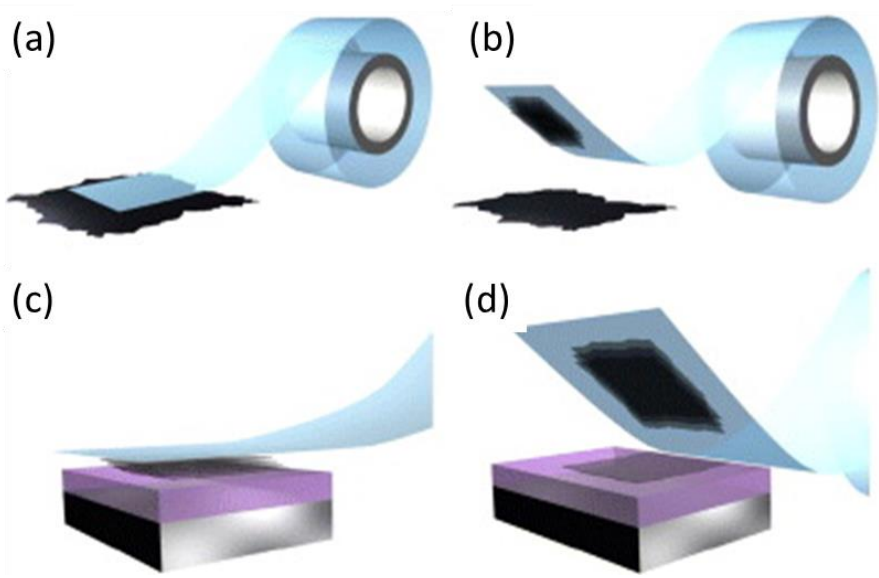

Figure. 1.5. Different steps of MLG fabrication by mechanical exfoliation.

1.3.3.2. Chemical exfoliation

To address scalability issues, chemical exfoliation techniques were later developed to create dispersions of layered compounds in solution that can then be deposited over very large areas [4]. Chemical synthesis of graphene starts from graphite, just like the mechanical exfoliation method. The general process is to take advantage of the intercalation of different chemical elements between graphite layers that can weaken van der Waals bonding. First, when graphite is immersed into concentrated sulfuric and nitric acid, graphite intercalation compounds (GIC) form, expanding the interspacing distance between graphite layers [54]. Subsequently, graphite sheets can be exfoliated by applying mechanical energy to the GIC's with an ultrasonicator [55,56]. To obtain single-layer graphene from graphite using this process, graphite oxide (GO) is used as a GIC. Hummer and Offeman synthesized a GO with sulfuric acid, sodium nitrate,

and potassium permanganate [57]. This GO was well dispersed in water owing to the electrostatic repulsion by intercalated hydroxyl and ether groups. After the deposition of the dispersed GO

onto a nonspecific substrate, a reduction process was followed, resulting in graphene sheets.

The advantages of this methods are as follows

- Higher output of production
- Economically competitive and convenient to manipulate

The disadvantages of the process are as follows

- Challenge to using this chemically derived graphene in electric applications because its electric properties are degraded due to the defects created during the oxidation and reduction processes.

1.3.3.3. Epitaxial growth on SiC substrate

A route toward wafer-scale graphene synthesis is the large-area, epitaxial growth of graphene on single crystalline SiC. As the graphene is directly prepared on this wide band gap semiconductor material, it is ideally compatible with industrial semiconductor processes. A number of different polymorphs of SiC, either 6H-SiC with AB stacking or 4H-SiC with ABC stacking, can be used for this type of epitaxial graphene growth. Both of these hexagonal forms of SiC have two different topmost layers along the c-axis, Si-face SiC and C-face SiC, which affect the morphology and quality of the resulting graphene differently [58].

Van Bommel et al. first developed the graphene synthesis through high-temperature annealing of SiC [59]. They found that thin graphite layers formed after heating SiC between 1000 °C and 1500 °C in ultrahigh vacuum (UHV) below 1040 Torr. The synthesis process involves three steps: the desorption of Si atoms from the SiC surface at high temperatures, subsequent surface reconstruction to a C-rich surface, and the formation of a conformal graphene layer initiated from islands at step edges (Fig. 1.6). The critical step in the synthesis process is to control the desorption rate of Si from the SiC surface. A single crystalline graphite layer is typically observed on the Si-face SiC, while in contrast, the C-face SiC shows a polycrystalline graphite layer with various in-plane orientations with respect to the lattice underneath.

The advantages of this methods are as follows

- High quality graphene.
- Easy method for growing single crystals of graphene.
- The layers of graphene can be controlled conveniently.

- Higher temperatures ensure reproducible, clean and ordered graphene.
- Patterning of graphene is easier due to the use of insulating SiC substrate.
- Further advantage is that SiC is already a large bandgap semiconductor already used in electronic applications.

The disadvantages of this methods are as follows

- MLG transfer process is difficult High temperature.
- Difficulty in growing uniform MLG in UHV conditions (impurity free conditions).
- Lattice constant mismatch and difference in coefficient of thermal expansion of SiC - C can lead to various defects.
- SiC crystalline substrate is expensive

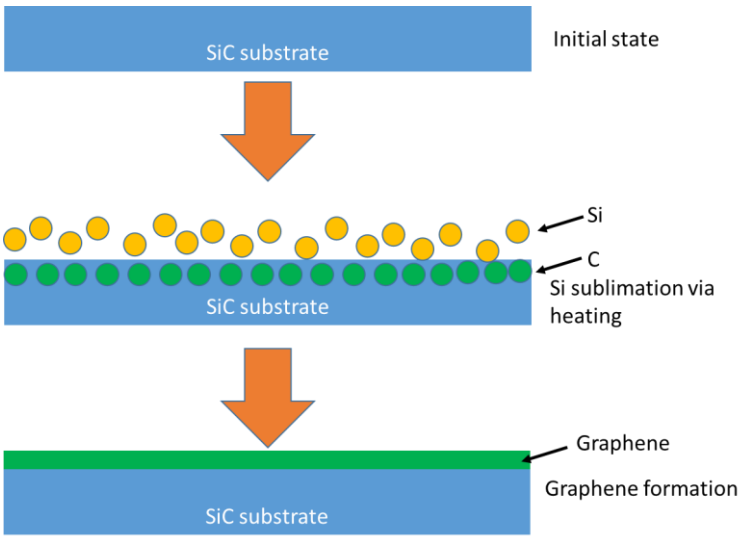

Figure 1.6. Process of an epitaxial growth on a SiC substrate. After the sublimation of silicon, carbon remains on the surface where it would be transferred to graphene later.

1.3.3.4. Chemical vapor deposition (CVD)

The most common technique for fabricating large area graphene is CVD. In CVD process, the graphene growth on a surface is caused due to thermal decomposition of molecules of a hydrocarbon gas (methane, ethanol, acetylene, propane etc) catalyzed by a metal surface or because of the segregation/precipitation of carbon atoms from the bulk metal [60]. Now a days, the widely used catalysts for the production of graphene and another allotropes of carbon such as carbon nanotubes are the transition metals. Figures 1.7(a) and (b) shows the schematic of thermal CVD process. In this process, a substrate is exposed to one or several precursor gases containing reactive elements. These elements are made to react by heating the chamber to high temperature.

In graphene CVD, typically three gases are introduced into the chamber. The primary atmosphere consists of Ar with a small amount of H_2. During the deposition phase, a carbon-containing gas is introduced to provide the material needed to grow the film. The Ar serves as a carrier gas to control the partial pressures of hydrogen and the carbon-containing gas. While the exact role of hydrogen in graphene CVD is not perfectly understood, it was suggested in reference [61] that H_2 serves several purposes. First, it helps the formation of sp^2 bonds. Second, it etches the weaker carbon-carbon bonds, assisting the formation of high quality bonds. Third, it reduces any oxide that may remain on the metal catalyst. The carbon-containing gas is almost completely decomposed at the high temperature used in graphene CVD (>1000 °C). Free carbon atoms attach to- and diffuse at the surface and form chemical bonds to each other. The sp^2 bonds are the most stable and thermodynamically favorable for carbon but the temperature, while high, is still too low for the efficient creation of a large-scale sp^2-hybridized carbon lattice. However, with the use of a metal catalyst as substrate, the energy barrier for creating such bonds is lowered and the film grows efficiently. The metal catalyst is essential for forming high quality bonds between the carbon atoms. As in many thin film deposition techniques, a high temperature and a low deposition rate favor high quality crystal growth. Therefore, the deposition temperature is kept close to melting point of the metal catalyst and the partial pressure of the carbon-containing gas is kept as low as possible.

The advantages of thermal CVD method for MLG fabrication are as follows

- High quality, impervious, and harder graphene is obtained.
- Producing large domains of graphene is easy.
- High growth rates possible.
- Good reproducibility.
- Comparatively cheaper for high quality graphene fabrication.

The disadvantages of CVD are as follows

- High temperatures (greater than 900 °C) leads to wrinkled graphene due to difference in Coefficient of Thermal Expansion.
- Complex process.
- Production of explosive and flammable H_2 gas.
- Difficulty in controlling the thickness in some cases (number of layers).
- Difficulty in transferring the film to other surface (exfoliation).
- Difficulty in achieving the uniform deposition of the carbon.

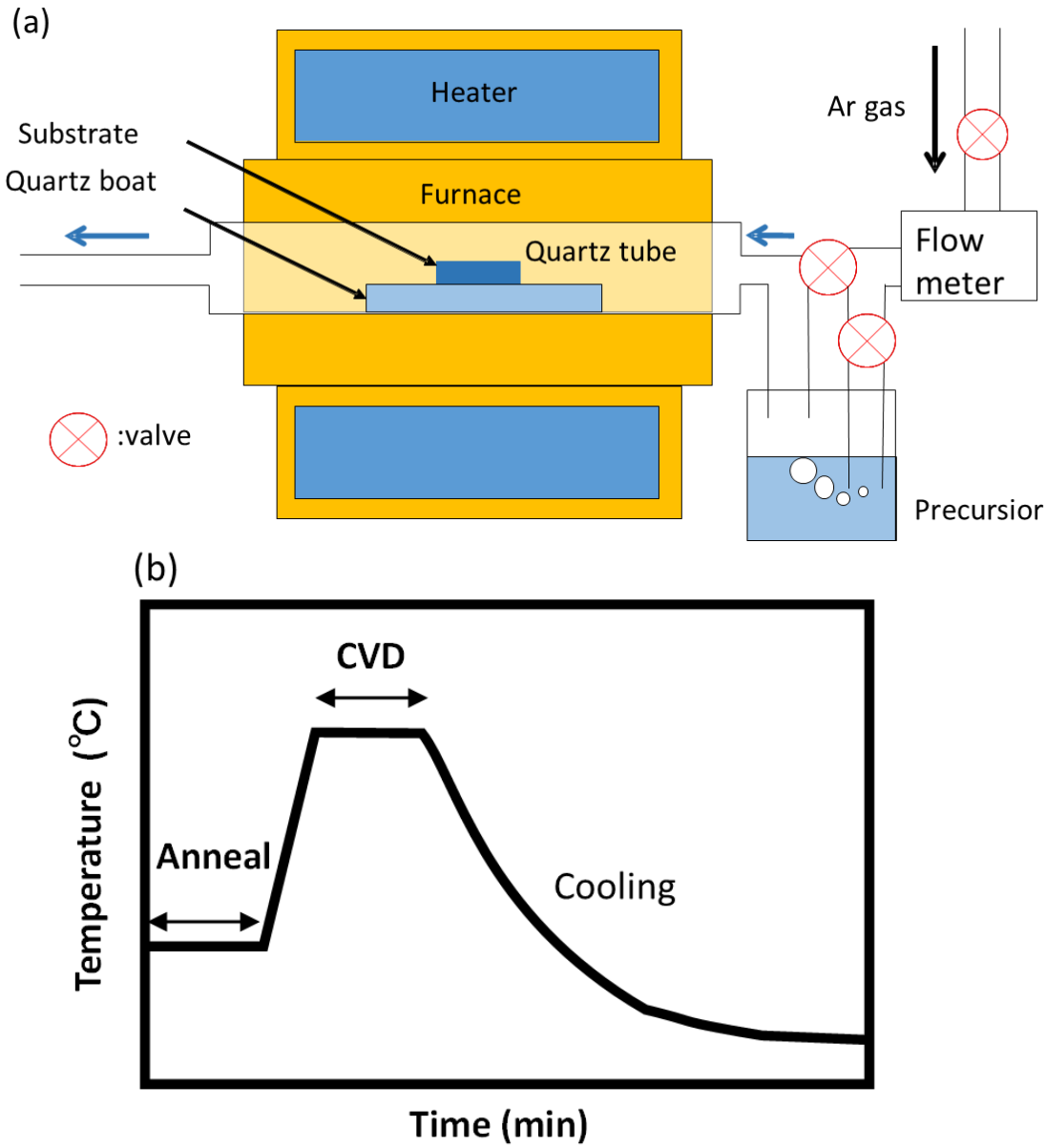

Figure 1.7. (a) Experimental set up and (b) the process of thermal CVD process.

1.3.3.5. Solid-phase reaction

Multilayer graphene deposition by solid phase reaction (SPR) is a process of transfer-free deposition of MLG onto a substrate. As it requires no transfer process, it is become popular day by day as direct MLG fabrication method [62-64]. In this method, amorphous carbon (a-C) is allowed to make reaction with a catalyst layer by a high temperature annealing. Upon cooling, MLG deposition by precipitation takes place at the both sides of the catalyst layer. The thickness of the MLG is directly proportional to the thickness of the a-C layer. This fabrication

method is the core of our thesis. The detailed of MLG fabrication by this method will be described in the next chapter.

1.3.3.6. Molecular beam epitaxy (MBE)

Molecular beam epitaxy is a technique which is widely used in materials research. It offers the possibility to synthesize a variety of materials (e.g. III-V semiconductors) on a large variety of templates, and at moderate temperatures (<1000 ^{o}C)[19]. MBE shows potential to overcome some drawbacks of the methods described above. One of its main advantages is thickness control, which in the context of graphene might enable the precise growth of not only mono- but also few-layer graphene films, as well as the direct growth of heterostructures. Since atomic species are used as the precursor, metallic substrates are not a mandatory requirement, and other technologically relevant substrates may be used. Another advantage of MBE is that in-situ methods may be used to directly monitor the films during growth.

1.3.4. Graphene applications

Graphene is a promising next-generation conducting material with the potential to replace traditional electrode materials such as indium tin oxide in electrical and optical devices [65]. It combines several advantageous characteristics including low sheet resistance, high optical transparency and excellent mechanical properties. Recent research has coincided with increased interest in the application of graphene as an electrode material in transistors, light-emitting diodes, solar cells and flexible devices.

Capability of graphene in handling current densities larger than 10^8 A/cm^2, low resistivity, and high thermal conductivity make it a potential material for interconnect applications [66].

Due to the extraordinary electronic properties, mechanical resistance and large specific surface area of graphene, another possible field of application is sensing [38]. The adsorption of molecules in the surface can modify the local charge carrier concentration and this can be detected in a Field Effect Transistor (FET) configuration. A single molecule detection has been achieved, which demonstrates the potential high sensitivity of graphene-based sensors [67].

Graphenes high electron mobility, outstanding optical properties and chemical and mechanical stability make it ideal for analog devices such as metal-semiconductor field effect transistor (MESFET) and high electron mobility transistor (HEMT) [68-70]. Unlike metal-oxide-semiconductor filed effect transistor (MOSFET), MESFETs and HEMTs do not involve an insulating layer; instead the switching is obtained in metal semiconductor junction. A major

concern of MESFET and HEMT is the need for thermally stable metal contacts that can survive local heating effect when the device is in operation. Thermally and mechanically stable graphene and MLG are good candidates for replacing conventional metal contacts which degrade easily at high temperatures by diffusing into semiconductors and forming undesirable ohmic contacts. The origin of high thermal stability of MLG is its high melting point.

Graphene/MLG can also be used as Schottky rectifier and its high barrier height and low reverse leakage current has been reported [29]. Due to its outstanding mechanical stability both graphene and MLG can be used as a Schottky rectifier with minimum degradation of diode properties when operating at high temperatures because of its high melting point.

The outstanding properties of graphene makes it suitable for further applications as listed below

Ultracapacitors and microbatteries: able to store big quantities of energy, 20 times more powerful than the current ones; and with a charging time 1000 times faster [38].

Bio-related material: biomedicine and biosystems like graphenecoated implants, biosensors, and drug delivery [38].

Thermal management material: high thermal conductivity, and consequently fast cooling [38].

Structural materials (paper, powder): much harder, stronger, and more flexible than current ones [38].

High performance computation: terahertz oscillators and high-speed field-effect transistors with switching speeds between 100 GHz and a few THz, and a performance 30 times higher than current [38].

Photovoltaics: more efficient solar cells by using graphene as a charge collector. Electrons in graphene which have been excited to a higher energy state by absorbing incoming light, transfer their energy to neighbouring electrons, rather than radiating it as photons [38].

Graphene based quantum dots: nanolight with extraordinary properties due to their remarkable quantum confinement and edge effects: systematic photoluminescent mechanisms, bandgap engineering, in addition to the potential applications in bioimaging, sensors, etc [38].

Graphene aerogel: is seven times lighter than air, and 12% lighter than the previous record holder (aero graphite). Its density is just 0.16 mg/cm3, and has a superb elasticity and absorption. It can recover completely after more than 90% compression, and absorbs up to 900 times its own weight in oil, at a rate of 68.8 g/s [38].

Optical modulators: are commonly used in communication and information technology to control intensity, phase, or polarization of light. Graphene allows broadband

light-matter interactions with ultrafast responses and can be readily pasted to surfaces of functional structures for photonic and optoelectronic applications [38].

1.4. Literature review related to the thesis

Since its discovery (2004), the number of publications related to graphene and graphene related materials are increased significantly. A large number of engineers and physicists are doing research on fabrication, characterization, and application of graphene and related materials. Figure 1.8 shows the scholarly output on graphene and related materials from 2004 to 2014.

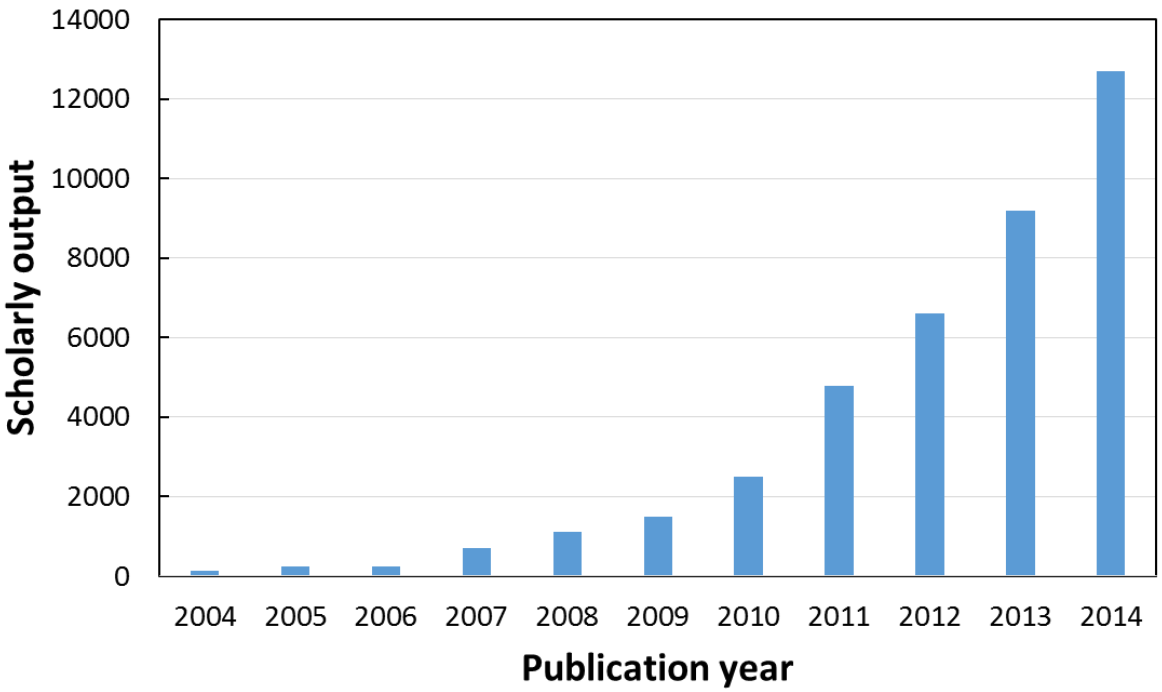

Figure 1.8. Research output on graphene and related materials from 2004 to 2014.

This section we will show some of the literature review related to out topic of interest briefly.

1.4.1. Literature review on fabrication and crystallinity improvement of MLG on dielectric substrate

K. Ueno et al [71]., studied on the effect of current stress during thermal CVD of MLG on Co catalytic layer and named their proposed CVD technique as current enhanced CVD (CECVD). Current stress varied from 2 to 10 A dc was applied during thermal CVD on their experiment. The final temperature of CVD was calculated to be the temperature including joule-heating during the experiment by measuring the sample temperature including joule heating. To show

the effect of current stress, same experiment was done by directly setting the furnace to the same temperature as was obtained with current stress in the previous experiment. They reported that the crystallinity of MLG obtained by CVD with current was higher than that without current at the same temperature as shown in Fig. 1.9. In their article, they also reported on the improvement of MLG crystallinity at a lower temperature for the interconnect applications by their proposed CECVD technique.

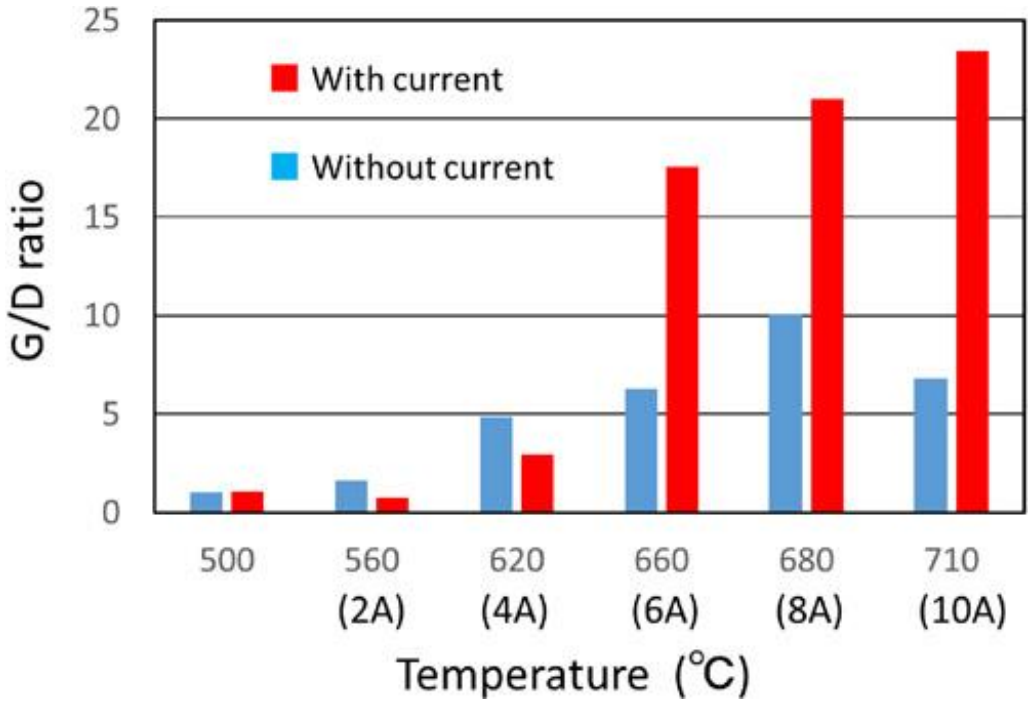

Figure 1.9. Plot of G/D ratio as a function of CVD temperature with and without current as shown in Ref. 71.

M. Zheng et al [72]., studied on metal-catalyzed crystallization of amorphous carbon to graphene. The experiment involved the deposition of a-C layer of thickness 2.5 to 40 nm on Si/SiO_2 substrate, followed by Ni thin film of thickness 100 to 300 nm. The samples were than annealed in a furnace at a temperatures between 650 to 950 ^oC. They reported the thickness of the MLG layer to vary directly proportional to the thickness of the a-C layer. They have reported the advantage of transfer-free deposition of MLG on dielectric substrate than the conventional CVD method.

M. Sato et al [62]., reported on MLG fabrication directly on SiO_2 substrate by annealing sputtered amorphous carbon with Co catalyst layer at the top. They have concluded with

successful fabrication of MLG on n-GaN substrate without complicated transfer process. The annealing temperature was 800 ^{o}C in their experiment.

M. Sato et al [63]., studied on the growth conditions for MLG obtained by annealing sputtered amorphous carbon. They used five different metal as catalyst for the growth of MLG on SiO_2. They have also changed the annealing medium for growth of MLG films. They reported that by optimizing the catalyst and the annealing gas, the resistivity of MLG can be decreased. They also reported the MLG grain size to be an important factor for the resistivity and the breakdown current in MLG interconnects and express the need of increasing the MLG grain size to not only decrease the resistivity but also increase the current tolerance of MLG wire.

M. Sato et al [64]., studied on intercalated MLG wires and metal/MLG hybrid wires obtained by annealing sputtered a-C. They have reported that the resistivity of the MLG can be lowered by optimizing the thickness of the catalyst and the sputtered a-C layer and the annealing temperature to stop the agglomeration of the catalyst layer. They have optimized the Co catalyst layer of thickness 400 nm for the formation of high crystalline MLG films without catalyst agglomerations. The optimized annealing temperature for high-crystalline and uniform MLG was 1200 ^{o}C.

L. A. Razak et al [73]., studied on the improvement of MLG quality by current stress during the thermal CVD. They have reported the enhancement of MLG crystallinity with the

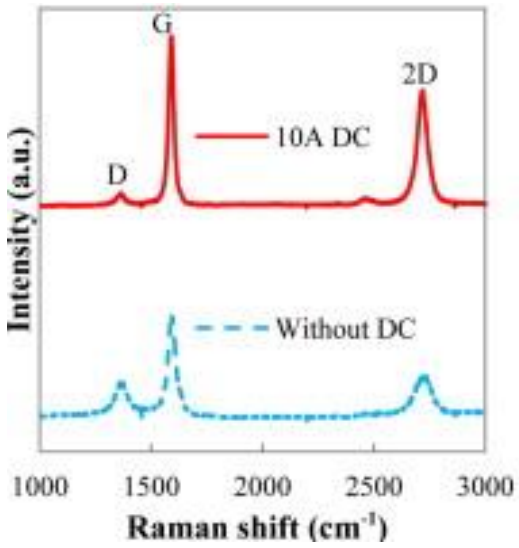

Figure 1.10. Raman spectra of MLG films deposited with and with current at the same CVD temperature. Image taken from Ref. 73.

increase of current density. The Raman spectra comparison for the MLG films deposited without current and with current enhanced CVD is shown in Fig. 1.10. The G/D ratio is seen

to be increased for the MLG films with current than those without current. They have also reported the better surface morphology of MLG on SiO_2 substrate can be achieved with current stress during CVD at comparatively lower temperature.

1.4.2. Literature review on fabrication and application of MLG on GaN substrate.

J. Sun et al [74]., studied on direct formation of large area carbon thin films on GaN by chemical vapor deposition without extra catalyst. They have used a high flow of NH_3 to stabilize the surface of the GaN surface during the deposition at 950 ^oC. Characterization of the thin films confirms that the thin films were sp^2 bonded, macroscopically uniform, and electrically conductive. This paper provides a roadmap for fabricating carbon based thin films such as graphene, MLG or carbon nanotubes for future transparent electrode on GaN.

Z. Yun et al [31]., studied on direct growth of graphene on GaN by using chemical vapor deposition without extra catalyst. They were succeeded in fabricating 5-6 layers of uniform graphene films by using CH_4 as the precursor. The CVD temperature was optimized to be 950 ^oC in their experiment for the fabrication MLG films with moderate crystallinity and uniformity. The graphene crystallinity as determined by G/D intensity ratio was found to be less than unity as was confirmed from the Raman spectra. From XRD measurement, they confirmed that the GaN layer was not affected by the high temperature CVD. In this article only fabrication of MLG was shown but no application was reported for the fabricated MLG films.

B. Wang et al [32]., studied on direct growth of graphene on GaN using C_2H_2 as carbon source. They were succeeded in fabricating 4-5 layers of graphene on n-GaN by using CVD method without using the extra catalyst. The effect of growth temperature on the growth of graphene films was systematically studied in their work. They have optimized the CVD temperature to be 830 ^oC. The G/D ratio of the MLG films were less than unity as was also observed in Ref. 40.

S. Tongay et al [30]., studied the rectification at graphene-semiconductor interface and reported the rectification property of graphene for various semiconductors like n-GaN, Si, GaAs, and SiC. In their experiment for device fabrication graphene was grown on Cu foil by thermal CVD and was transferred to GaN substrate. Since the rectification effect observed in a wide variety of semiconductors, they suggested a number of applications including sensors, or to MOSFET and HEMT devices. They suggested that graphene is applicable for such

applications because of its mechanical stability, its resistance to diffusion, its robustness at higher temperatures, and its demonstrated capability to embrace multiple functionalities.

S. Kim et al [29]., studied the electrical characteristics of graphene Schottky contacts formed on n- GaN semiconductor. Graphene was also grown on Cu foil and transferred to GaN for the fabrication of the device similar to Ref. 43. They found excellent rectifying behavior with a rectification ratio of ~ 10^7 at ±2 V with reverse leakage current of 1 x 10^{-8} A/cm^2 at -5 V. The Schottky barrier height (SBH) as determined by thermionic emission (TE) model, Richardson plots, and barrier inhomogeneity model, were 0.90, 0.72 and 1.24 eV, respectively. They reported the much larger barrier height was attributed to the presence of large number of surface states and the internal spontaneous polarization field of GaN, resulted in a significant upward band bending. They have summarized graphene as a promising candidate for use as a Schottky rectifier in the n-type GaN semiconductor.

S. Tongay et al [75]., studied qualitatively the stability of graphene/GaN diodes at elevated temperatures. They found the rectification property of graphene upto 550 K and the rectification property vanishes above 650 K. Upon cooling, the diode shows excellent recovery with improved rectification. They summarized the reason of thermal stability of the graphene-GaN diode as the graphene layer can be acted as an impenetrable diffusion barrier layer against Au. Finally they suggested the potential application of graphene into high-performance analog device operating at elevated temperatures.

1.5. Aim of our present study

In our current research, we have concerned on fabrication of MLG for on SiO_2 for interconnect applications and MLG on n-GaN for electrode application. It has been reported that graphene/MLG interconnects leads to higher current endurance [76,77]. For power device applications, high current endurance material is required for high current density [78]. This is why we have fabricated MLG both for interconnect and electrode applications.

For the application of MLG as an interconnect material transfer-free deposition with improved crystallinity is more promising. Lowering the deposition temperature and uniformity over the entire substrate is another prerequisite for the application of MLG as interconnect.

For a high performance GaN based device for high-temperature and high frequency applications such as MSM ultraviolet (UV) light photo-detectors, MESFETs, HEMTs, MOSFETs, HBTs and Schottky rectifier diodes , it requires a thermally stable Schottky contact that does not degrades in high temp. applications. Graphene/MLG-n-GaN diodes are extensively studied and its high barrier height and low reverse leakage current has been

investigated by several groups [29,30], and expected high thermal stability due to high melting point and thermally stable structural behavior of graphene/MLG. In Refs. 29 and 30, the fabrication of the diode is done by transferring MLG from Cu foil to n-GaN which is not ideal for many applications.

For thermally stable diodes with better performance transfer-free deposition is preferable. Several research groups [31,32] reported the transfer-free deposition of MLG on n-GaN by thermal CVD. But, the deposition temperature were as high as 950 ^{o}C and the MLG crystallinity was not good as the D peak intensity was higher than the G peak intensity. Moreover, there is no report on the fabrication of MLG based device with transfer-free deposition of MLG on n-GaN.

From the literature reviews in previous Sect. and the above discussion, the objective of our present study can be summarized as follows

- To fabricate MLG films directly on dielectric substrate which requires no transfer process with improved crystallinity and uniformity by solid-phase reaction (SPR) since, MLG deposition by SPR has an advantage of transfer-free deposition on the substrate [62-64]. The lowering of fabrication temperature is also our objective.

- To fabricate MLG films directly on n-GaN substrate with improved crystallinity and uniformity as compared to the previous work. We ought to decrease the fabrication temperature to minimize the carbon diffusion through GaN.

- To fabricate a Schottky barrier diode with transfer-free deposition of MLG on n-GaN and to study the electrical characteristics of the fabricated diode.

- To study the thermal stability of the electrical characteristics of fabricated diodes and to compare with a conventional diode.

- To study the electrical characteristics of the fabricated diode by changing the top metal contact.

1.6. Our approach to reach the goal

For the transfer-free deposition of MLG on SiO_2 as well as n-GaN substrate our strategy is to fabricate MLG by SPR. To improve the crystallinity of MLG films on SiO_2 by SPR, a new approach of current stress application during annealing of carbon doped cobalt (Co-C) layer was used. For the graphitization of a-C by SPR, energy is needed. In previous reports [62-64],

energy was supplied only by heating the sample at high temperatures. In our present research we have supplied energy by flowing current through the sample. We were expecting to provide the total energy as a combination of heat and current. Current stress application during thermal CVD can improve the crystallinity of MLG films significantly and has been reported [71, 73] and expected the same improvement by SPR. To improve the uniformity of MLG an additional Cu layer on the Co-C layer as capping was used to stop agglomeration of Co.

To improve the crystallinity and uniformity of MLG on n-GaN by SPR a new approach of heat-sputtering for the deposition of C and Co were used to reduce the thermal expansion among C, Co and GaN. The heat-sputtered C/Co layer is expected to reduce the thermal expansion difference when annealed at a higher temperature for SPR to occur.

1.7. Structure of the thesis

The flowchart of this dissertation is shown in Fig. 1.11. This thesis is organized in seven chapters as follows

Chapter-1 consists of the background and objectives of the thesis. Some explanation about graphene/MLG, its discovery, properties, and applications are given in this chapter. The important review of some previous works related to the thesis are also given in the current chapter. The goal of our present work as well as the structure of the thesis is also discussed in the present chapter.

Chapter-2 consists of the details discussion on MLG fabrication by SPR. The MLG characterization techniques such as Raman spectroscopy, SEM, TEM, optical microscopy, laser microscopy, and four point probe method for measuring sheet resistance are also described in this chapter.

Chapter-3 consists of transfer-free fabrication technique of MLG on SiO_2 substrate with improved crystallinity and uniformity at comparatively lower temperature by SPR. The MLG characterizations with and without current at the same temperature by taking account the temperature rise due to joule heating are discussed in this chapter. The formation of uniform MLG on SiO_2 using a Cu capping layer is also presented and discussed in this chapter.

Upon confirming the formation of MLG film by SPR with improved crystallinity and uniformity on SiO_2, we expect the formation of MLG on n-GaN substrate by SPR. **Chapter-4** consists of fabrication and characterization of nanocarbon (NC) films directly on n-GaN substrate without extra catalyst by solid-phase reaction. The crystallinity of the NC films were poor and the deposition temperature was as high as 1000 ^{o}C.

To improve the crystallinity and decrease the fabrication temperature, Co layer as catalyst was used over a-C for SPR to occur. **Chapter-5** consists of fabrication and characterization of MLG films directly on n-GaN substrate with improved crystallinity and uniformity by SPR with Co as catalyst. The effect of heat sputtering for the deposition of a-C and Co in comparison with room temperature (RT) sputtering has been discussed. The reason behind crystallinity and uniformity improvement is also described in this chapter.

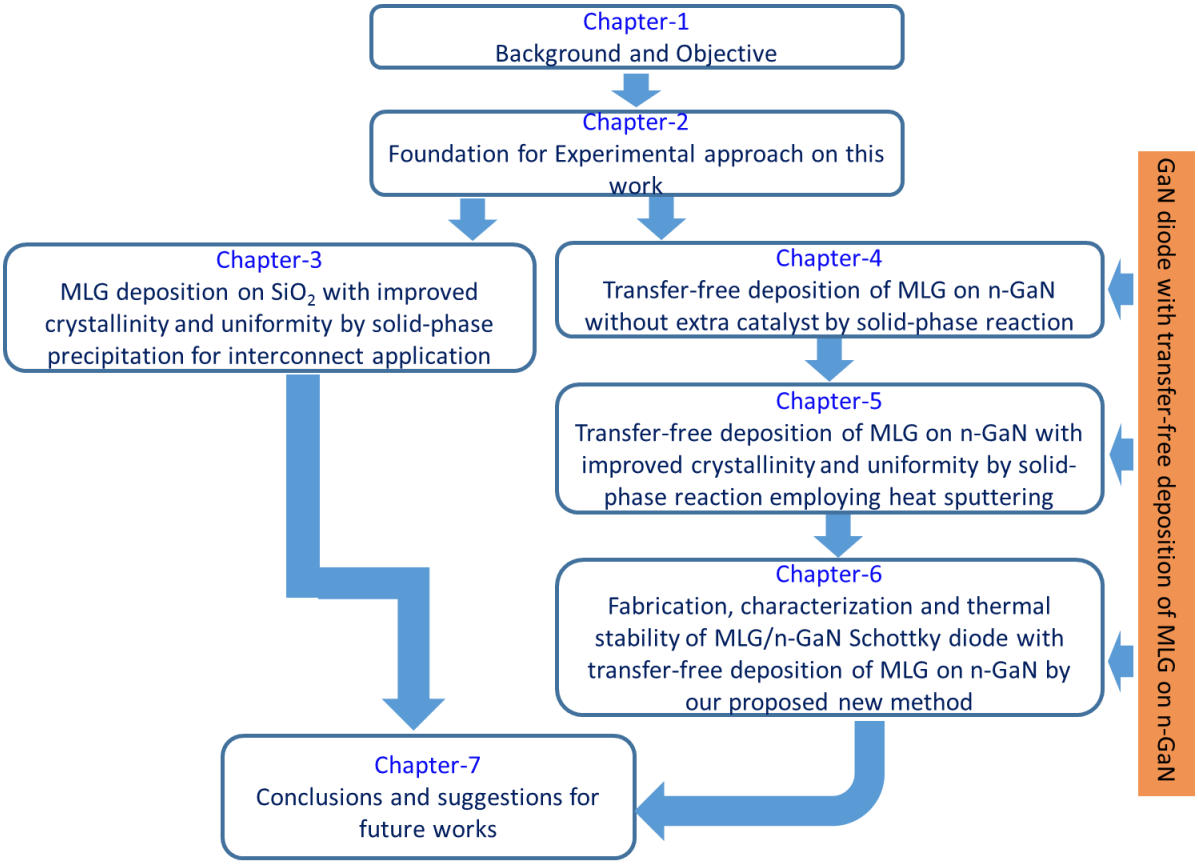

Figure 1.11. Flowchart of the dissertation.

For the application of the MLG films deposited by our new method as described in the previous chapter, MLG-GaN SBD was fabricated with transfer-free deposition of MLG by our new method. **Chapter-6** consists of fabrication and characterization of MLG/n-GaN Schottky diode with transfer-free deposition of MLG on n-GaN as described in the previous chapter. The thermal stability of the fabricated device is also presented and compared with a conventional Ni/n-GaN diode in this chapter. The seris resistance of the MLG/n-GaN diode was found to be larger in comparison with Ni/n-GaN diode. To reduce the series resistance, the top metal was changed from Au to Cu and the characteristics of Cu/MLG/n-GaN diode was studied. It was

found that there was a small variation of series resistance between Au/MLG/n-GaN and Cu/MLG/n-GaN diodes. Finally, the top contact metal of the diode was changed from Au to Au/Ni and the electrical properties were compared.

Chapter- 7 summarizes all the results in the thesis. The conclusion of our present work is also given. Some aspect of future work is also given in this chapter.

Reference of each chapter is given at the end of each chapters.

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CHAPTER TWO
GRAPHENE / MLG FABRICATION AND CHARACTERIZATION

2.1. Overview

The purpose of this study is transfer-free deposition of MLG on dielectric (SiO_2) and semiconducting (n-GaN) substrate with improved crystallinity and uniformity at a comparatively lower temperature. Different MLG fabrication techniques, advantages and disadvantages of each fabrication technique is described in the previous chapter. From the study of advantages of various fabrication technique in the previous chapter, it was found that MLG deposition by solid-phase reaction (SPR) has an advantage of transfer–free deposition on the desired substrate. In this context, we select SPR as the MLG fabrication technique on both SiO_2 and n-GaN substrate. The details of MLG fabrication by SPR is described in this chapter. Various characterization technique of MLG are also discussed in this chapter.

2.2. Details of MLG deposition by solid-phase reaction (SPR)

Upon reviewing the previous works on graphene or MLG in the previous chapter, we have already known that the transfer-free MLG fabrication on substrate is promising for the fabrication of a device. Upon studying the advantages and disadvantages of various MLG fabrication techniques as discussed in the previous Sect., we found that transfer-free MLG fabrication is still a challenge. MLG fabrication by SPR requires no transfer process as a result, we can fabricate MLG as well as MLG based device without transfer by this method. The main purpose of selecting SPR is firstly to avoid the transfer step and secondly, to compare the performance of an MLG based semiconductor device fabricated by our method with MLG transfer based one.

MLG deposition by SPR involving the following steps.

- Substrate cleaning
- Sputtering
- Annealing
- Co removing

The process flow of fabrication is shown in Fig. 2.1.

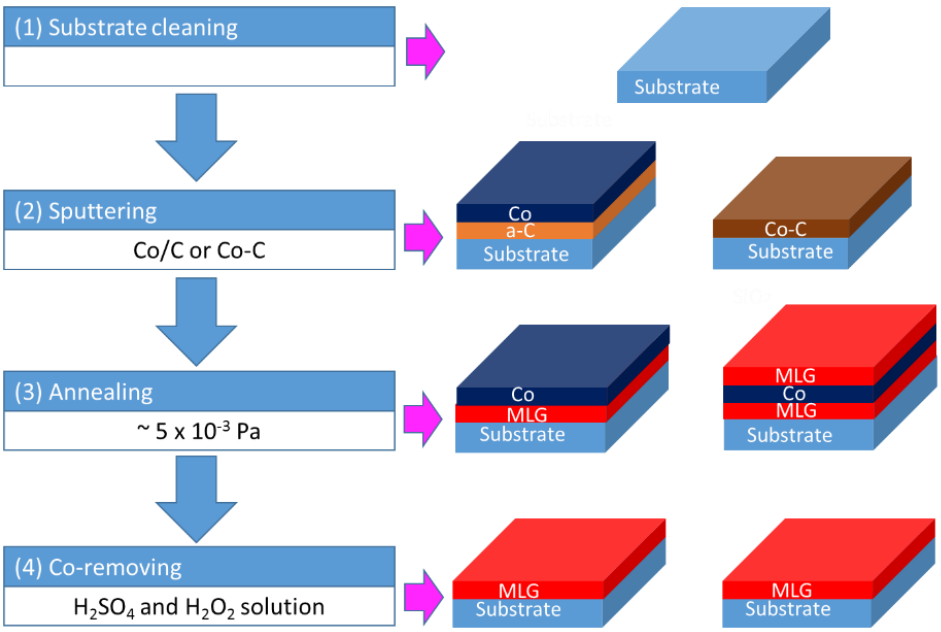

Figure. 2.1. Different steps of MLG fabrication by solid-phase reaction.

2.2.1 Substrate cleaning

Two types of samples were used in our experiment for the fabrication of MLG are SiO_2 and n-GaN. The cleaning steps for the two samples were differen

Cleaning of SiO_2 substrate

- The substrates were cleaned ultrasonically in a solution consists of H_2SO_4 and H_2O_2 with ratio 3:1 (120 : 30 ml).
- The substrates were then cleaned with ultrapure water.
- The substrate surface were dried first with flow of N_2 and then on a hot plate at 110 ^oC for 10 minutes.

Cleaning of GaN substrate

- The n-GaN substrates were cleaned ultrasonically with tetramethylammonium hydroxide (TMAH), isopropyl alcohol (IPA) and ultrapure water.
- The substrates were then dipped in concentrated HCl for 1 minute to remove the native oxide layers and then again cleaned in ultrapure water ultrasonically and finally dried in nitrogen flow.

2.2.2. Sputtering

Sputtering is a widely used method for the deposition of metallic thin films. The basic process is as follows. A target, or source of the material desired to be deposited, is bombarded with energetic ions, typically inert gas ions such as Argon (Ar+). The forceful collision of these

ions onto the target ejects target atoms into the space. These ejected atoms then travel some distance until they reach the substrate and start to condense into a film. As more and more atoms coalesce on the substrate, they begin to bind to each other at the molecular level, forming a tightly bound atomic layer. One or more layers of such atoms can be created at will depending on the sputtering time, allowing for production of precise layered thin-film structures. By using this magnetron sputtering a-C and Co layers were deposited onto our desired substrate. The pressure was 1 Pa with a base pressure of 7 x 10^{-4} Pa. The sputtering power for Co and C was 100 and 400 W respectively. The basic mechanism of magnetron sputtering is shown in Fig. 2.2. The sputtering set-up in our laboratory is shown in Fig. 2.3.

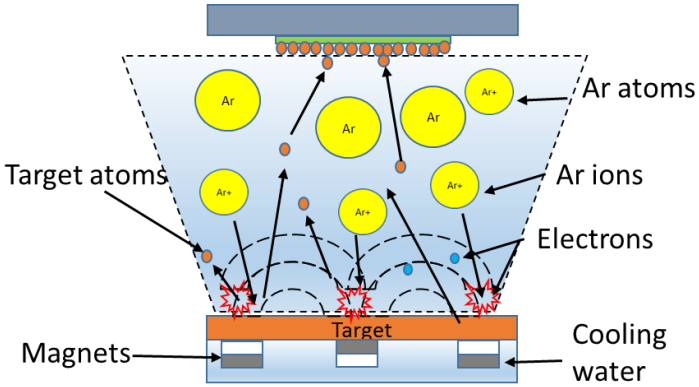

Figure 2.2. Basic components of a magnetron sputtering. Ionized Ar bombards the target releasing atoms that produce layer on substrate.

Figure 2.3. The magnetron sputtering set-up in our laboratory (SHIBAURA).

2.2.3. High vacuum annealing

In this step the sputtered sample is inserted inside a tube furnace. The annealing temperature was between 600 and 800 ^{o}C. The annealing time was 30 min inside the furnace in a pressure

of 5 x 10^{-3} Pa. After annealing the sputtered structure was allowed to cool down to room temperature. During annealing a reaction between Co and a-C should take place and during cooling the carbon precipitates at the both sides of the catalyst to form MLG. The sequences of annealing is shown in Fig. 2.4.

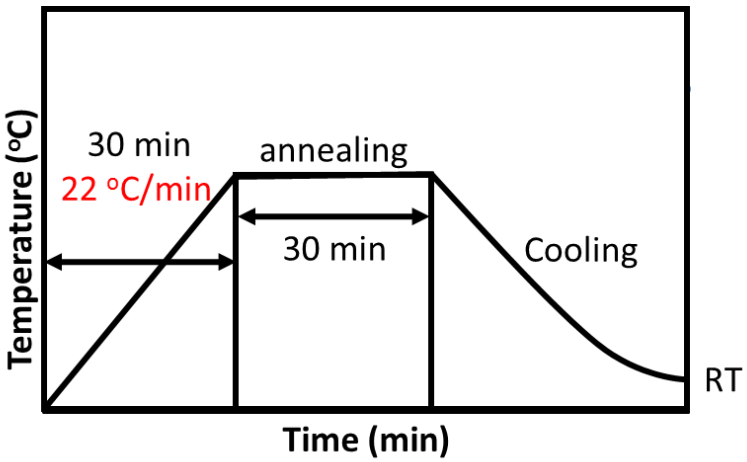

Figure 2.4. Temperature profile for MLG deposition by SPR.

2.2.4. Co removing

The last step of the experiment is removing the Co layer from the top of the MLG layer. For the removal of cobalt a solution consist of 100 ml water, 90.4 µl H_2SO_4 and 184 µl H_2O_2 was used. The removing time was 3 min. The annealed substrates were dipped in the solution using a rubber band and a pin set. After completing the removal of Co, MLG was cleaned in ultrapure water and dried at 110 °C for 5 min. The Co removing procedure is shown in Fig.2.5.

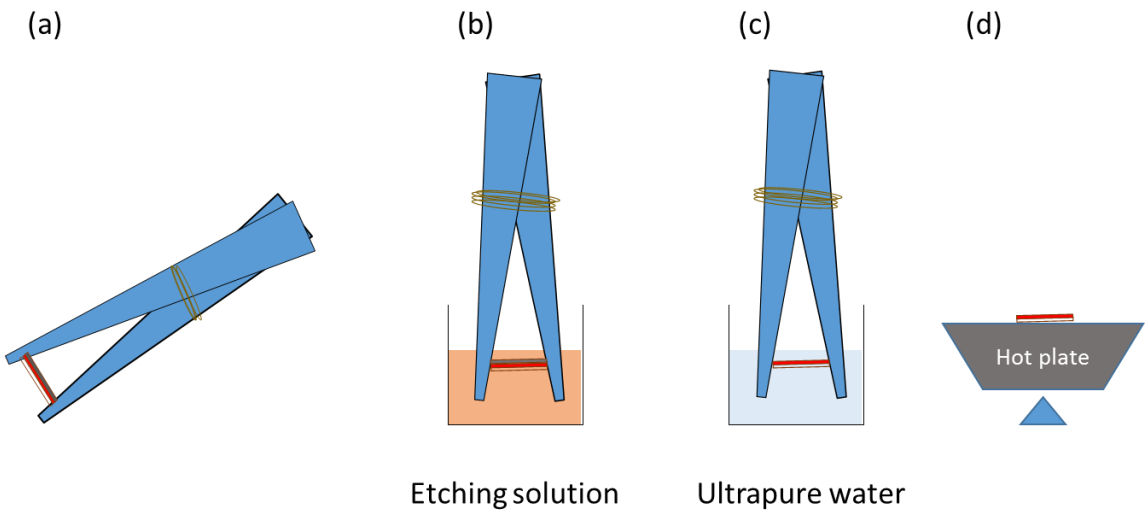

Figure. 2.5. Different steps of Co removal.

2.3. Graphene/MLG characterization

2.3.1 Raman spectroscopy

Raman spectroscopy is the most powerful and non-destructive method for the identification and characterization of nanocarbon materials. Not only graphene or MLG but also other nanocarbon materials such as carbon nanotube, diamond like carbon, amorphous carbon, and carbon fullerenes can be characterized by Raman spectroscopy.

It is known that interaction of light with matter provide rapid, quantitative, non-destructive, characterization of materials. Raman spectroscopy is based on inelastic scattering arising from electron-phonon interactions. Incoming electromagnetic waves interact with quantized lattice vibrations by polarizing the electron distributions in atomic bonds. In other words, the incident light makes the electron cloud to oscillate, which in turn causes the atoms to vibrate. This interaction with the lattice vibrations absorbs or augments the energy of the electrons depending on the available vibrational modes and quantum selection rules. When the electrons finally relax and scatter a photon, it will have a different energy than the incident photon. The resulting change in frequency, known as the Raman shift, provides characteristic information about the atomic constitution, bonding character, and impurity concentration of the material.

Figure 2.6 illustrates the Raman scattering mechanism. Diagrammatically, we see that the incident light is absorbed by the molecule or bond, promoting it into a virtual excited state. Statistically, the system will return to the initial state in a radiative process known as Rayleigh scattering, however, some probability exists that it will relax to a different state by coupling to an optical phonon. If the final state has more energy than the ground state (phonon is created), the emitted photon is red shifted (Stokes shift). Less likely, is a transition from which the electron cloud gains energy (phonon is annihilated) and emits a blue shifted photon (anti-Stokes shift). Since the probability of phonon creation and annihilation is determined by Bose-Einstein statistics, the relative intensity of the shifts is proportional to: [1]

$$\frac{I_S}{I_{\alpha-S}} \propto \frac{n+1}{n} = \exp(\frac{E_p}{k_B T}) \qquad (2.1)$$

Where, n is the number of phonons with energy, Therefore, barring certain cases where quantum selection rules or photoluminescent interference precludes its use, Stokes Raman is preferable due to the higher signal intensity. Finally, if the incident excitation energy coincides with an electronic transition, then the process is resonant and the intensity is enhanced.

The electron-phonon interaction is analogous to the classical damped, forced, harmonic oscillator, where the damping energy is related to the polarizability, and the driving force is equivalent to the oscillating electric field created by the incident light. For perturbatively damped systems such as this, the resulting peaks approach Lorentzian functions, with line widths that are inversely proportional to the phonon lifetime [2]. The peak intensity is a complex function of the polarizability, which itself is time-dependent and a function of the vibrational mode.

Raman spectra are plotted as the intensity of the scattered light versus the Raman shift in inverse wavenumbers (cm^{-1}). Lasers are commonly used as excitation sources because they are monochromatic and their intensity makes up for low scattering probabilities. Very efficient notch or edge filters are used to block the Rayleigh scattered light so that high-gain photodetectors can be used to capture low intensity Raman features. Raman is a low probability process that is best suited to study surfaces like graphene. Surface sensitivity can be tuned somewhat by the choice of incident radiation, while quantum selection rules determine the coupling cross-sections for interactions between specific incident wavelengths and the vibrational modes of the lattice. Three characteristic Raman peaks are generally used to investigate the thickness, crystalline size, defect density, and doping level of graphene: the G-band (1580 cm^{-1}), the D-band (1350 cm^{-1}), and the 2D-band (2700 cm^{-1}).

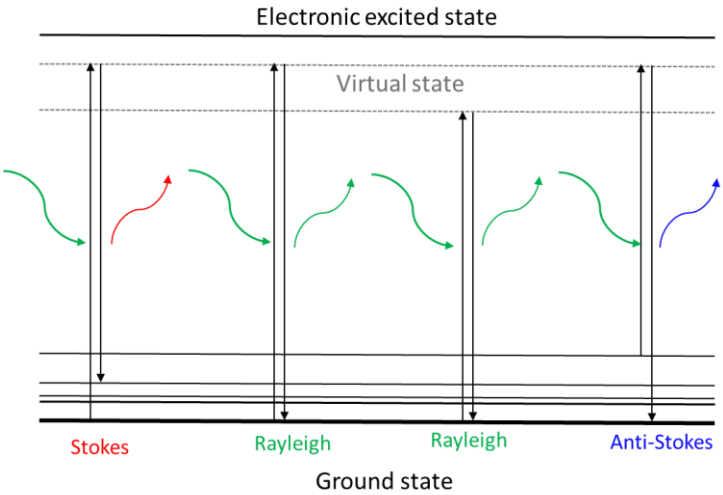

Figure 2-6. Diagram of the Raman scattering process. Incident radiation causes the electron cloud to oscillate, thereby promoting the system into a virtual excited state. The system typically relaxes back to the initial state, emitting a photon of equal energy, in a process known as Rayleigh scattering. In rare cases, the oscillating electron cloud will lose (gain) energy by coupling to an allowed vibrational mode of the system and scatter a red (blue) shifted photon.

- The G band appears at ~1580 cm^{-1}. This peak corresponds to the high-frequency E_{2g} phonon at the center of Brillouin zone, which corresponds to in-plane vibrations of sp^2 carbon atoms. Although the intensity increases with the number of graphene layers, the intensity of one monolayer graphene is surprisingly comparable to the bulk graphite signal.
- The D band is located at ~1350 cm^{-1}. The phonon mode responsible of this peak is related to the breathing modes of the sp^2 six-atom rings and their excitation is forbidden for the Raman fundamental selection rules. D band can only appear in the presence of defects or in the edges of a graphene flake. That is why it is called the defective band and is usually used as a measure of the quality of the graphene flakes. It comes from transverse optical phonons around the Brillouin zone corner K [3], it is active by double resonance [4,5], and is strongly dispersive with excitation energy [6], due to a Kohn anomaly at K. [7]
- Finally, the 2D band, at ~2700 cm^{-1}, is the second order effect of the D band and it does not need the presence of defects or edges for its activation. To this 2D band relies most of the graphene characterization because its shape and intensity strongly depend on the number of graphene layers. [8]

The origin of the differences in the 2D band while increasing the number of layers, is the appearance of multiple vibration modes when, in spite of having one monolayer of graphene, the measured sample has several layers. In multilayer graphene the D band is the result of the addition of two peaks and the 2D band results from the addition of four different peaks. The shape of the 2D band changes because of the relative intensity of these peaks varies depending on the number of the layers. Hence, graphene monolayer has a very narrow 2D band with intensity roughly four times greater than those of the G band whereas increasing the number of graphene layers makes the 2D/G intensity ratio decrease and the 2D band becomes broader and upshifted [8]. The various modes of Raman spectra and its significance is shown in Table 2.1.

Since, the three Raman bands for the characterization of MLG appears within the Raman shift (cm^{-1}) between 1000 to 3000 cm^{-1}, In this thesis Raman measurement was carried out within the Raman shift ranging from 1000 to 3000 cm^{-1}. The Raman measurements were carried out to measure the crystallinity of MLG films as the MLG crystallinity is determined by G/D peak intensity ratio [9]. Higher G/D ratio corresponds to higher crystallinity. The MLG grain

size can also be determined from the G/D ratio using Raman spectra. The general equation to determine the G/D ratio can be written as [10],

$$L_a(nm) = (2.4 \times 10^{-10})\lambda_l^4 \left(\frac{I_D}{I_G}\right)^{-1} \quad (1)$$

Where L_a is the MLG grain size, λ_l is the wavelength of the excitation laser used in raman measurement and I_D and I_G belongs to thearea intensity of the D and G peak.

Raman measurement was also carried out for the mapping of the non-uniformly deposited MLG films over the substrate to trace the position of MLG on the substrate.

Table 2.1. Different modes of Raman spectra and its significance.

Mode	Position (cm^{-1})	Significance
G	~1580	This band comes from graphitic structure and the intensity of the peak increases with number of graphene layers
D	~1350	This band comes from the defect structure such as edges and grain boundaries
2D	~2700	This is the second order effect of the D band and is used to determine number of graphene layers

2.3.2. Optical microscopy (OM)

Optical microscope is a device that magnifies the object image by visible light with the help of a number of lenses. This microscopes are sometime termed as light microscope. This microscopes are widely used for magnification of small objects. Optical microscopes are the oldest design of microscope and were possibly invented in their present compound form in the

17th century. Basic optical microscopes can be very simple, although there are many complex designs which aim to improve resolution and sample contrast.

The image from an optical microscope can be captured by normal light-sensitive cameras to generate a micrograph. Originally images were captured by photographic film but modern developments in CMOS and charge-coupled device (CCD) cameras allow the capture of digital images. Purely digital microscopes are now available which use a CCD camera to examine a sample, showing the resulting image directly on a computer screen without the need for eyepieces. Figure 2.7 (a) shows the diagram of a compound optical microscope.

A compound microscope uses a lens close to the object being viewed to collect light (called the objective lens) which focuses a real image of the object inside the microscope (image 1). That image is then magnified by a second lens or group of lenses (called the eyepiece) that gives the viewer an enlarged inverted virtual image of the object (image 2) [11].

The use of a compound objective/eyepiece combination allows for much higher magnification. Common compound microscopes often feature exchangeable objective lenses, allowing the user to quickly adjust the magnification [11]. A compound microscope also enables more advanced illumination setups, such as phase contrast. In this work, the optical microscope was used to take the enlarged photos to view the surface of the deposited film.

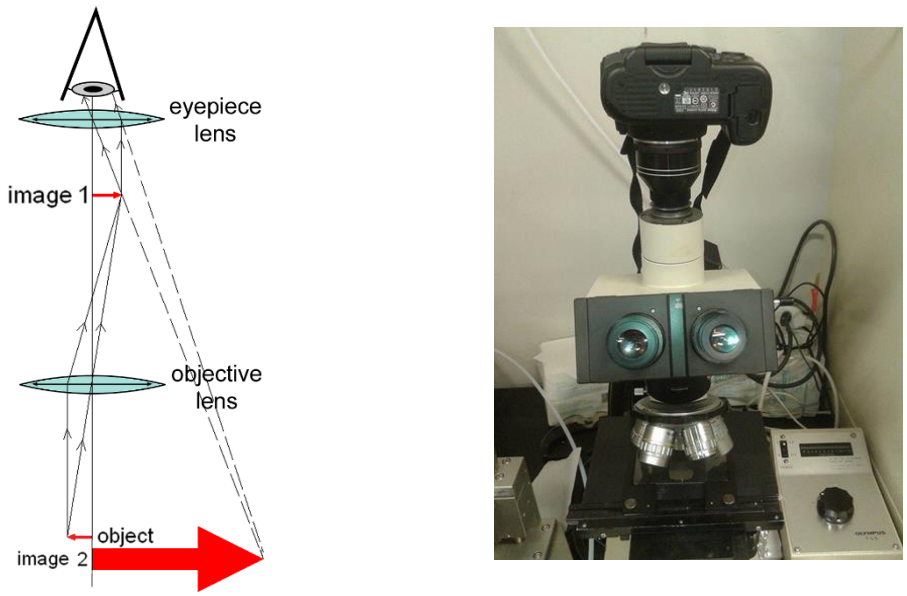

Figure 2.7. (a) Diagram of a compound microscope and its magnification procedure and (b) the optical microscope set-up in our laboratory to view the image in a camera (OLYMPUS, Japan)

2.3.3. Scaning electron microscopy (SEM)

A scanning electron microscope (SEM) is used to take the image of a very small samples with higher magnification then optical microscope. SEM is a type of electron microscope that produces images of a sample by scanning it with a focused beam of electrons. The electrons interact with atoms in the sample, producing various signals that give information about the sample's surface topography and composition. The electron beam is generally scanned in a raster scan pattern, and the beam's position is combined with the detected signal to produce an image. SEM can achieve resolution better than 1 nanometer. Specimens can be observed in high vacuum, in low vacuum, in wet conditions (in environmental SEM), and at a wide range of cryogenic or elevated temperatures.

The most common SEM mode is detection of secondary electrons emitted by atoms excited by the electron beam. The number of secondary electrons that can be detected depends, among other things, on specimen topography. By scanning the sample and collecting the secondary electrons that are emitted using a special detector, an image displaying the topography of the surface is created.

In a typical SEM, an electron beam is thermionically emitted from an electron gun fitted with a tungsten filament cathode. Tungsten is normally used in thermionic electron guns because it has the highest melting point and lowest vapor pressure of all metals, thereby allowing it to be electrically heated for electron emission. Another reason is the low cost.

The electron beam, which typically has an energy ranging from 0.2 keV to 40 keV, is focused by one or two condenser lenses to a spot about 0.4 nm to 5 nm in diameter. The beam passes through pairs of scanning coils or pairs of deflector plates in the electron column, typically in the final lens, which deflect the beam in the x and y axes so that it scans in a raster fashion over a rectangular area of the sample surface.

When the primary electron beam interacts with the sample, the electrons lose energy by repeated random scattering and absorption within a teardrop-shaped volume of the specimen known as the interaction volume, which extends from less than 100 nm to approximately 5 µm into the surface [12]. The size of the interaction volume depends on the electron's landing energy, the atomic number of the specimen and the specimen's density. The energy exchange between the electron beam and the sample results in the reflection of high-energy electrons by elastic scattering, emission of secondary electrons by inelastic scattering and the emission of electromagnetic radiation, each of which can be detected by specialized detectors. Figure 2.8 shows (a) signals emitted from different parts of the interaction volume in a SEM and (b)

schematic of an SEM. The beam current absorbed by the specimen can also be detected and used to create images of the distribution of specimen current. Electronic amplifiers of various types are used to amplify the signals, which are displayed as variations in brightness on a computer monitor (or, for vintage models, on a cathode ray tube). Each pixel of computer video memory is synchronized with the position of the beam on the specimen in the microscope, and the resulting image is therefore a distribution map of the intensity of the signal being emitted from the scanned area of the specimen [13]. In older microscopes images may be captured by photography from a high-resolution cathode ray tube, but in modern machines they are digitized and saved as digital images.

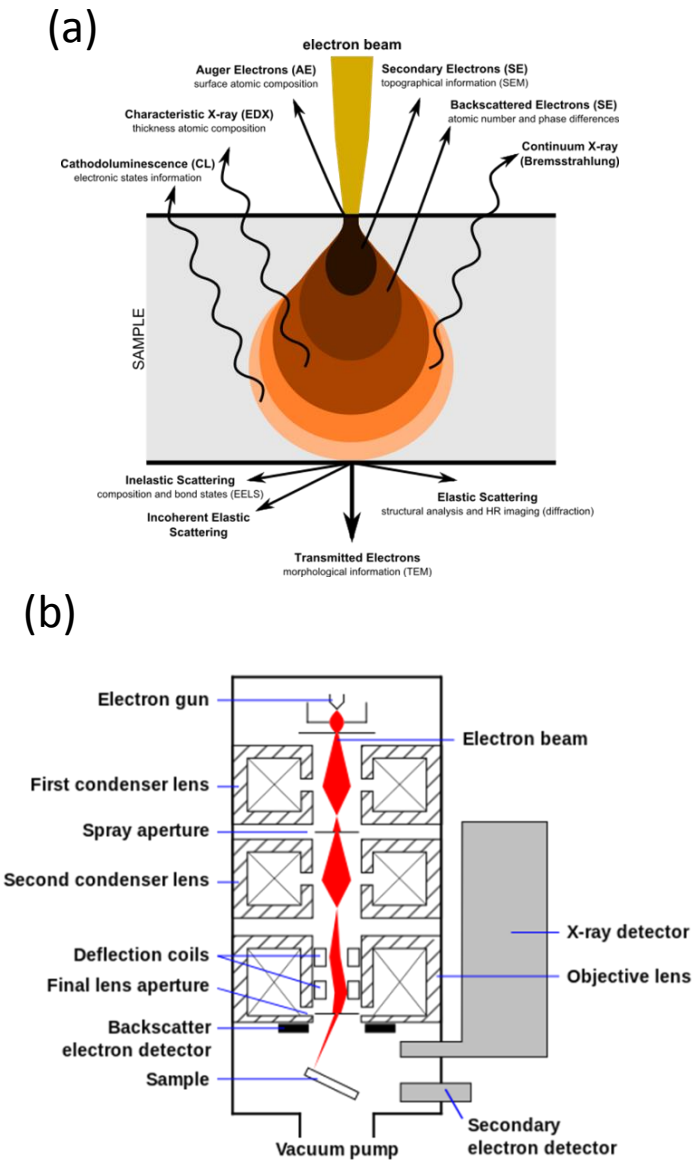

Figure 2.8 (a) Signals emitted from different parts of the interaction volume in a SEM and (b) schematic of an SEM, image [13].

In this thesis, FE-SEM was used to characterize the surface of the deposited films to view the surface image with a much higher magnification than optical microscope. The composition and uniformity of the sample surface were also determined by SEM.

2.3.4. Transmission electron microscopy (TEM)

Cross-sectional TEM image is the most important analysis method to measure the film thickness, film quality, growth condition, and interface condition. Fig. 2.9 Shows TEM system. The images in a TEM is formed by two main stages.

Stage A is the scattering of an incident electron beam by a specimen. This scattered radiation passes through an objective lens, which focuses it to form the primary image.

Stage B uses the primary image obtained in stage A and magnifies this image using additional lenses to form a highly magnified final image. In the process of forming the primary image the objective lens produces a diffraction pattern at its back focal plane. The diffraction pattern is a Fourier transform of the scattered electron wave. The primary image is the Fourier transform of the diffraction pattern. This two-step process forms the basis of image formation during high-resolution transmission electron microscopy (HRTEM). The high-resolution image is, in effect, an interference pattern of the beams formed at the back focal plane of the objective lens.

In this thesis TEM was used to take the cross-sectional image of our MLG films. The thickness of the MLG films as well as information about the growth mechanism was obtained by cross-sectional TEM image.

2.3.5. Laser microscopy

In this form of optical microscopy, the focused beam of a laser is scanned over the sample and the reflected intensity is displayed as a function of position to create a digital reflected light image of the sample. Scanning a focused laser beam allows the acquisition of digital images with very high resolution since the resolution is determined by the position of the beam rather than the pixel size of the detector. Laser Scanning Microscopy (LSM) and Confocal LSM (CLSM) permit a wide range of qualitative and quantitative measurements on difficult samples. These measurements include topography mapping, extended depth of focus, and 3D visualization (red/blue). Because Si and GaAs are transparent in the near infra-red, imaging can be done through the wafer backside using an infra-red laser, often without thinning. Using the stepping motor of the stage, a high resolution composite image of a large planar surface can be easily obtained.

In this thesis, laser microscopy was used to measure the uniformity of the MLG surface. We have also measured the thickness of MLG layer for patterned MLG structure on a substrate.

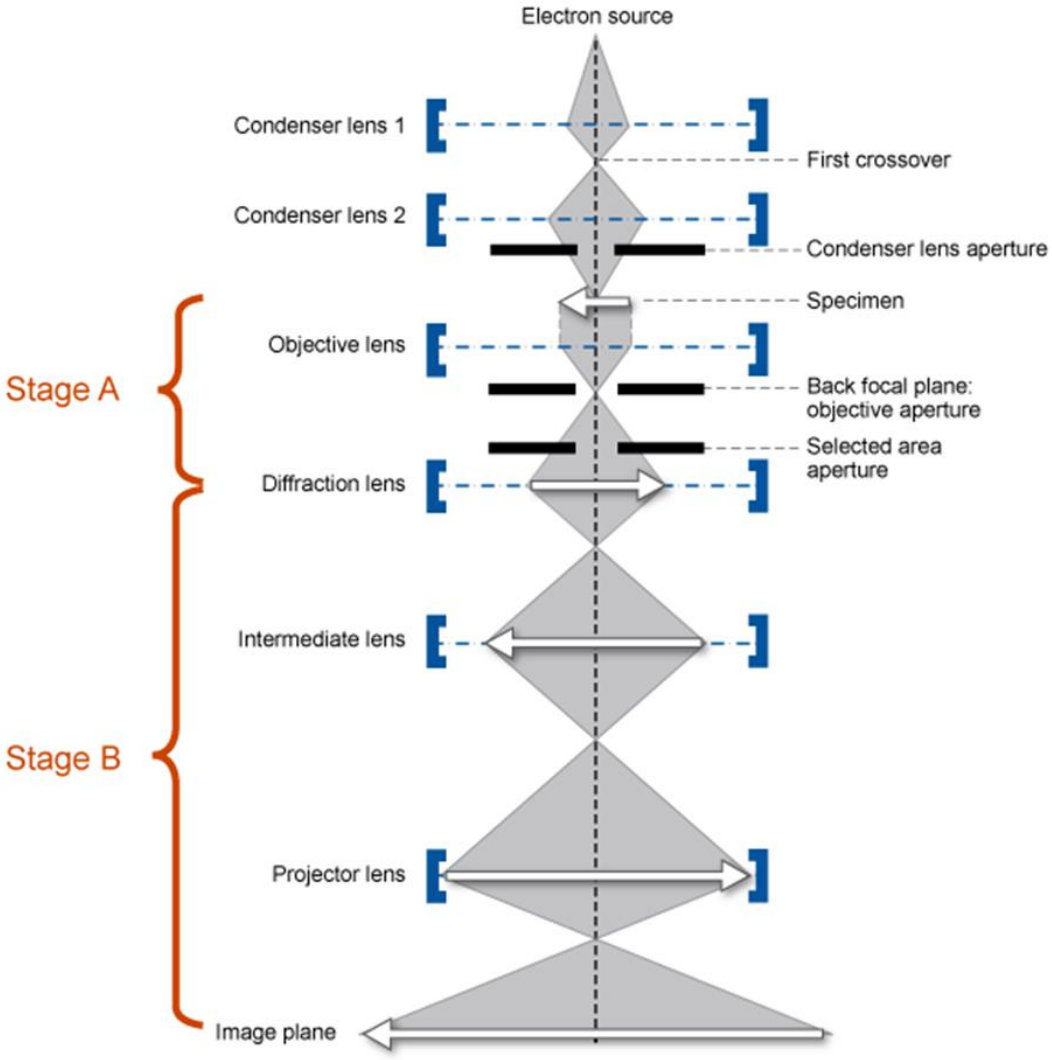

Figure. 2.9. Schemetic of a TEM with two stage magnification. Image " Australian microscopy and microanalysis research facility (ammrf)"

2.3.6. X-ray diffractometer (XRD)

X-ray powder diffraction (XRD) is a rapid analytical technique primarily used for phase identification of a crystalline material and can provide information on unit cell dimensions. The analyzed material is finely ground, homogenized, and average bulk composition is determined.

X-ray diffraction is based on constructive interference of monochromatic X-rays and a crystalline sample. These X-rays are generated by a cathode ray tube, filtered to produce monochromatic radiation, collimated to concentrate, and directed toward the sample. The

interaction of the incident rays with the sample produces constructive interference (and a diffracted ray) when conditions satisfy Bragg's Law ($n\lambda=2d \sin \theta$). This law relates the wavelength of electromagnetic radiation to the diffraction angle and the lattice spacing in a crystalline sample. These diffracted X-rays are then detected, processed and counted. By scanning the sample through a range of 2θangles, all possible diffraction directions of the lattice should be attained due to the random orientation of the powdered material. Conversion of the diffraction peaks to d-spacings allows identification of the mineral because each mineral has a set of unique d-spacings. Typically, this is achieved by comparison of d-spacings with standard reference patterns.

Figure 2.10. XRD measurement system (Rigaku/Rint-TTRIII).

X-ray diffractometers consist of three basic elements: an X-ray tube, a sample holder, and an X-ray detector. X-rays are generated in a cathode ray tube by heating a filament to produce electrons, accelerating the electrons toward a target by applying a voltage, and bombarding the target material with electrons. When electrons have sufficient energy to dislodge inner shell electrons of the target material, characteristic X-ray spectra are produced. These spectra consist of several components, the most common being K_α and K_β. K_α consists, in part, of $K_{\alpha1}$ and $K_{\alpha2}$. $K_{\alpha1}$ has a slightly shorter wavelength and twice the intensity as $K_{\alpha2}$. The specific wavelengths are characteristic of the target material (Cu, Fe, Mo, Cr). Filtering,

by foils or crystal monochrometers, is required to produce monochromatic X-rays needed for diffraction. $K_{\alpha 1}$and $K_{\alpha 2}$ are sufficiently close in wavelength such that a weighted average of the two is used. Copper is the most common target material for single-crystal diffraction, with CuKα radiation = 1.5418Å. These X-rays are collimated and directed onto the sample. As the sample and detector are rotated, the intensity of the reflected X-rays is recorded. When the geometry of the incident X-rays impinging the sample satisfies the Bragg Equation, constructive interference occurs and a peak in intensity occurs. A detector records and processes this X-ray signal and converts the signal to a count rate which is then output to a device such as a printer or computer monitor.

The geometry of an X-ray diffractometer is such that the sample rotates in the path of the collimated X-ray beam at an angle θ while the X-ray detector is mounted on an arm to collect the diffracted X-rays and rotates at an angle of 2θ. The instrument used to maintain the angle and rotate the sample is termed a goniometer. For typical powder patterns, data is collected at 2θ from ~5° to 90°, angles that are preset in the X-ray scan. Fig. 2.10 shows a photograph of our XRD measurement system.

We have used XRD to determine various phases of the annealed structure. We have also used XRD spectra to determine the reaction occurring at the sample during annealing at high temperatures.

2.3.7 Four point probe technique

The sheet resistance of our various sample after deposition by sputtering was measured by four point probe technique to determine the uniformity of the samples.

The four-point probe technique is one of the most common methods for measuring the semiconductor resistivity because two-point probe method is difficult to interpret. The sheet resistance is calculated form potential difference between inside 2 terminals (between B probe and C probe) after applying the current between outside 2 terminals (between A probe and D probe) as shown in Fig. 2.11. The resistance by two-probe technique is higher than accurate resistance because it includes the contact resistance (R_C) between metal probe and semiconductor surface and spreading resistance (R_{SP}) of each probe. Neither R_C nor R_{SP} can be accurately calculated so that semiconductor resistance (R_S) cannot be accurately extracted from the measured resistance. On the other hand, four-probe technique can neglect these parasitic resistances because the current value which flows between terminals is very small and potential drop can be disregarded. In this study, sheet resistance was measured by four-probe technique.

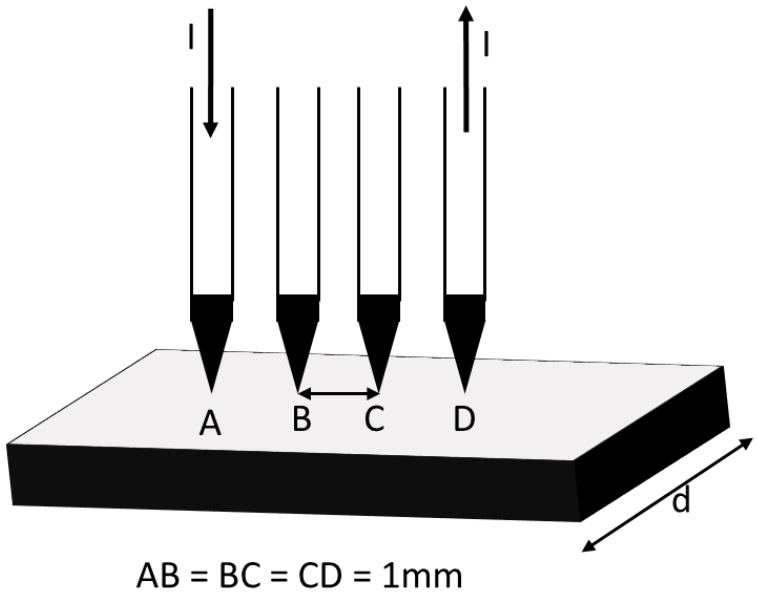

Figure 2.11. Illustration of four point probe system.

For an arbitrarily shaped sample the sheet resistance (R_{sh}) is given by

$$R_{sh} = \frac{V}{I} * CF \qquad 2.2$$

Where, CF is correction factor that depends on the sample geometry. If the distance among probes (s; in this study, s=1 mm) is greatly shorter than the width of a sample (d), CF equals to $\pi/\ln(2)=4.53$.

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CHAPTER THREE
EFFECT OF CURRENT STRESS ON FORMATION AND CRYSTALLINITY OF MULTILAYER GRAPHENE ON SiO_2 BY SOLID-PHASE REACTION

3.1. Background and objectives

Multilayer graphene (MLG) is considered to be the new candidate material for narrow interconnects owing to its potentially lower resistivity [1,2], higher thermal conductivity [3,4], and higher current carrying capacity [5,6] than Cu. In a short time since its first development, there have been great achievements in fabrication and applications of MLG for narrow interconnects that probably will soon have an impact in today's consumer society. MLG with higher crystallinity is a prerequisite for application in narrow interconnects. Several methods have been proposed for the fabrication of MLG films, such as exfoliation from highly oriented pyrolytic graphite (HOPG) [7], high-temperature decomposition of SiC substrates [8-10], thermal chemical vapor deposition (CVD) on metal catalysts such as Ni [11,13], Co [14], and Cu [15-17], conversion from solid carbon sources [18-20] and annealing sputtered amorphous carbon by solid-phase reaction (SPR) [21-23].

CVD is commonly used for low-cost fabrication of MLG, but MLG cannot be fabricated directly onto a substrate by this method, and transfer of MLG is required for interconnect application [24]. Also by CVD, a thick catalytic layer is required to stop agglomeration [25]. MLG fabrication by SPR has the advantages of direct deposition on a dielectric substrate and nonrequirement for a transfer process [22]. M. Sato et al [21-23], studied on the direct growth of MLG on SiO_2 substrate by annealing sputtered amorphous carbon below a catalyst layer. They have reported that the annealing temperature as high as 1200 ^oC and the catalyst layer of 240 nm thickness were required to stop agglomeration for the deposition of uniform MLG on SiO_2. The annealing temperature should be reduced to minimize the C diffusion through the substrate during annealing. Therefore, synthesis of MLG films with higher crystallinity at a comparatively lower temperature with good uniformity over the substrate is a critical challenge for interconnect application.

L. A. Razak et al [26] and K. Ueno et al [27] studied on the effect of current stress on the formation and crystallinity of MLG by thermal CVD on SiO_2 substrate. They have reported that the crystallinity of MLG was affected by applying current stress during thermal CVD.

They have considered the temperature rise of the samples due to Joule heating throughout their experiment and set the final temperature of the sample as the temperature including Joule heating effect. They compared the crystallinity of two MLG films deposited by thermal CVD at same temperature but one with current stress and the other without current stress and reported the significant improvement of crystallinity of the current stress applied sample than those without current. Therefore, it is established that applying current stress during thermal CVD can improve the crystallinity of MLG significantly.

In this study, our objective is to fabricate MLG films directly on SiO_2 substrate with improved crystallinity and uniformity by SPR. Decreasing the fabrication temperature is another challenge of this study. The main approach to reach the goal is to apply a current stress during annealing of a carbon doped Co (Co-C) layer. The effect of current stress on the formation and crystallinity of MLG films will be determined by comparing the crystallinity between two MLG films deposited with and without current stress at the same temperature deposition including joule heating.

3.2. Experimental methods

3.2.1. Sample preparation

The experimental setup and the process flow of MLG fabrication are shown in Figs. 3.1. As the substrate, SiO_2/Si wafers were cut into 2 × 1.5 cm^2. The substrates were cleaned ultrasonically in a solution containing H_2SO_4 and H_2O_2 with a ratio of 3:1. The substrates were then cleaned in ultrapure water properly. Then the substrates were exposed to flow of nitrogen and finally, the substrates were dried on a hot plate at 110 ^oC for 10 min. A Co-C layer of 100 nm thickness on the SiO_2/Si substrate was deposited by magnetron sputtering. The percentage of C in Co was 20 at. %. For the formation of crystalline and uniform MLG on SiO_2 by SPP, the optimized C percentage in Co-C is 20 as was reported by S. Sano et.al. [28]. The concentration of C in Co was adjusted by changing the load and tune of the RF target for the deposition of C. The sputtering condition for C and Co were adjusted such that within the exactly same sputtering time 100 nm Co-C layer deposited with 20% of C in Co. The flow rate of Ar was 20 sccm and the pressure was 1 Pa with a base pressure of 7.00 × 10^{-4} Pa. The sputtering powers for Co and C were 100 and 400 W, respectively. The structure of the sputtered film was Co-C/SiO_2/Si. After deposition of Co-C layer, the sheet resistance of the deposited films were measured to confirm the uniformity of deposition.

The effect of current stress was investigated by comparing the crystallinities of MLG films annealed at the same temperature without and with current. To do so, the temperature

properties of the furnace were determined. First, the furnace was set at a certain temperature and current was applied. Owing to Joule heating, the temperature of the sample was higher than the set furnace temperature. The temperature of the sample including Joule heating was measured using a thermocouple placed on the sample surface and recorded. Secondly, the final temperature including Joule heating was directly set in the furnace for preparing another sample without current stress. By this way, we can prepare two sets of MLG films at the same temperature but with and without current. The annealing time was 30 min in vacuum at 8×10^{-3} Pa. Various annealing temperatures between 600 and 800 ^{o}C and current stresses between 2 and 10 A dc were used. For annealing with current stress, first the sample was inserted into the furnace and the furnace was set to the desired temperature. As soon as the furnace reached the set temperature, dc current was set to flow; after 30 min the furnace as well as the current were switched off and the sample was allowed to cool to room temperature. During the annealing period a SPR of C and Co should take place and during the cooling of the sample the C atoms precipitates and the formation of MLG takes place. Figure 3.2 shows the experimental set-up in our laboratory for annealing with current stress.

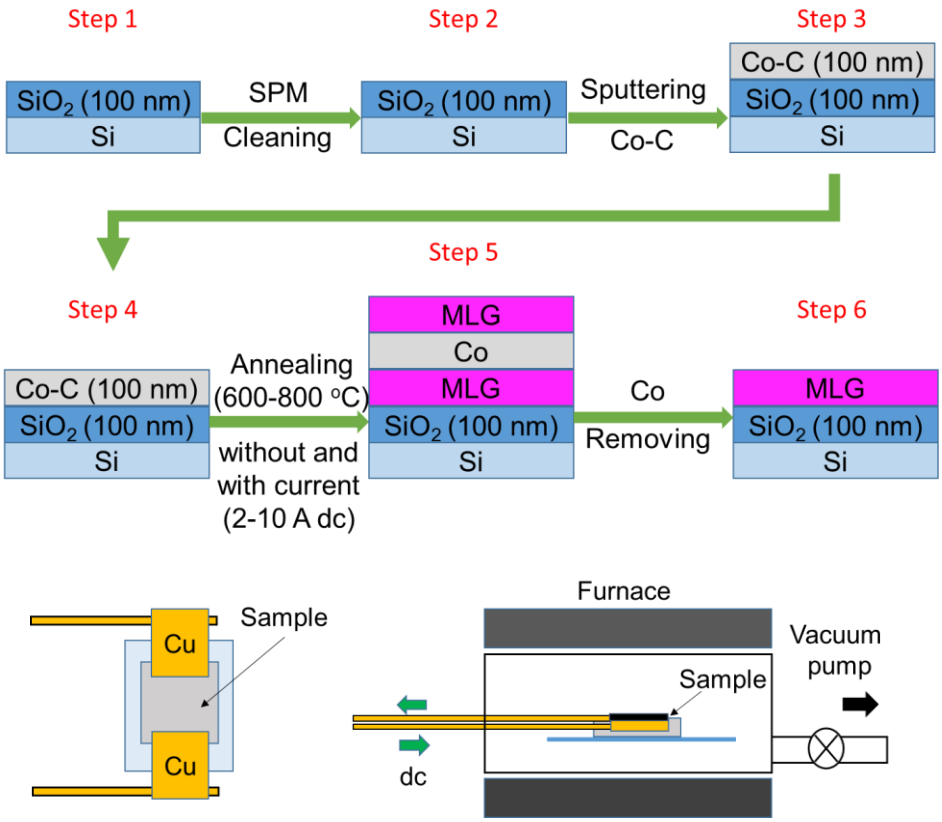

Figure 3.1. Fabrication of MLG directly on SiO_2 substrate: experimental setup for annealing with current stress and process flow of fabrication of MLG.

The Co layer from the top of the MLG layer was removed by a solution of volume 100 ml with 90.5 µl of H_2SO_4 and 184 µl of H_2O_2. The etching time was 2 – 3 min. After the removal of Co, the MLG films were cleaned by dipping the sample in ultrapure water and finally it was dried on a hot plate at 110 ^oC for 5 min.

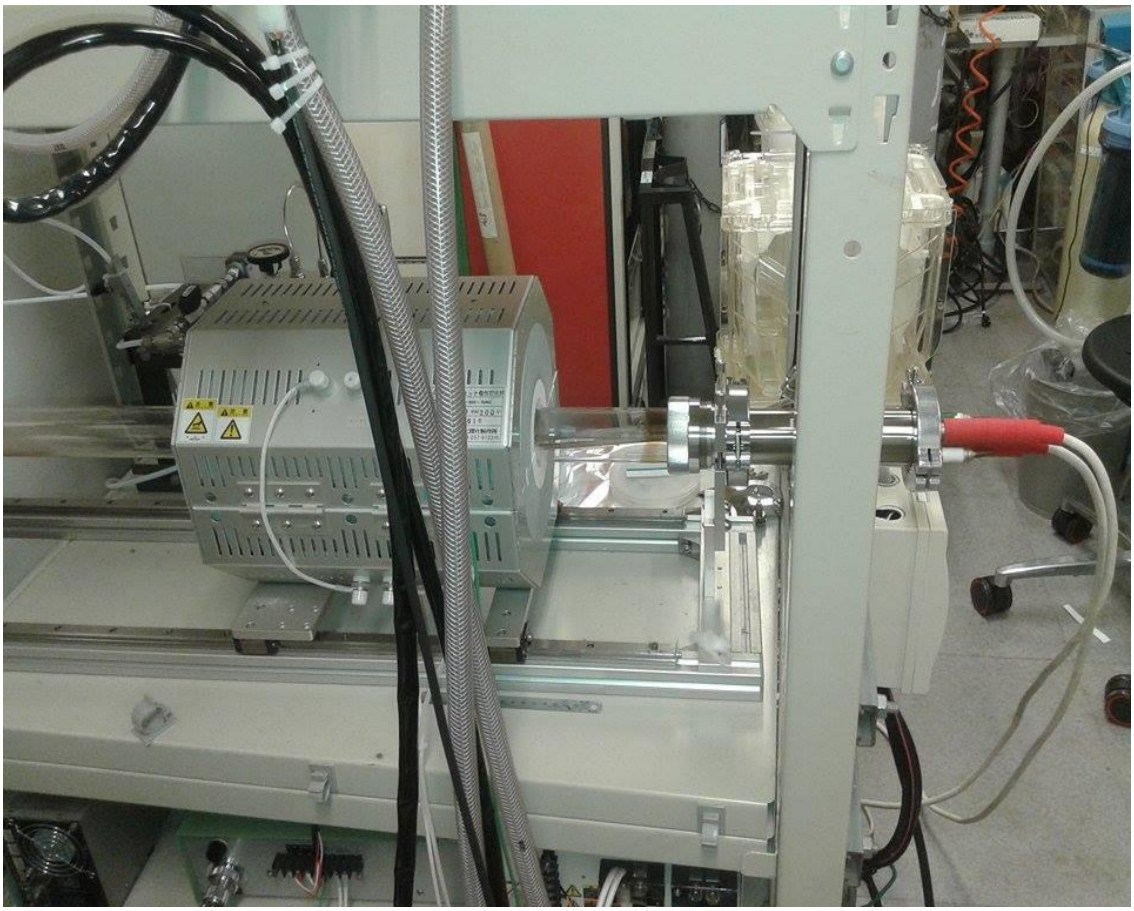

Figure 3.2. Experimental arrangement for annealing with current stress.

To investigate the effect of joule heating, the temperature property of the furnace was determined for fixing the annealing temperature of the sample. To do that, firstly the furnace temperature was set at 600 ^oC and current stresses of 2, 3, 5, 7, and 10 A were applied across the sample. The actual temperature of the sample during annealing including the joule heating was recorded by placing a thermocouple in contact with the sample surface. The temperature of the samples during annealing with current stress was found to be larger than the set temperature of the furnace. The average temperature of the sample during annealing was the average temperature recorded by the thermocouple. The temperature property of the furnace is summarized in Table 3.1. From Table. I, the rise of temperature of the sample are seen to be

increased proportionally with current stress. If we consider the set temperature to be 600 ^{o}C with 2 A current, the annealing temperature of the sample is 638 ^{o}C. The variation of temperature increase with current stress is shown in Fig. 3.3.

Table 3.1. Temperature rise of the sample with various current stresses due to Joule heating.

Set temperature with dc stress	Temperature of sample
600 ^{o}C + 2 A	638 ^{o}C
600 ^{o}C + 3 A	680 ^{o}C
600 ^{o}C + 5 A	721 ^{o}C
600 ^{o}C + 7 A	758 ^{o}C
600 ^{o}C + 10 A	800 ^{o}C

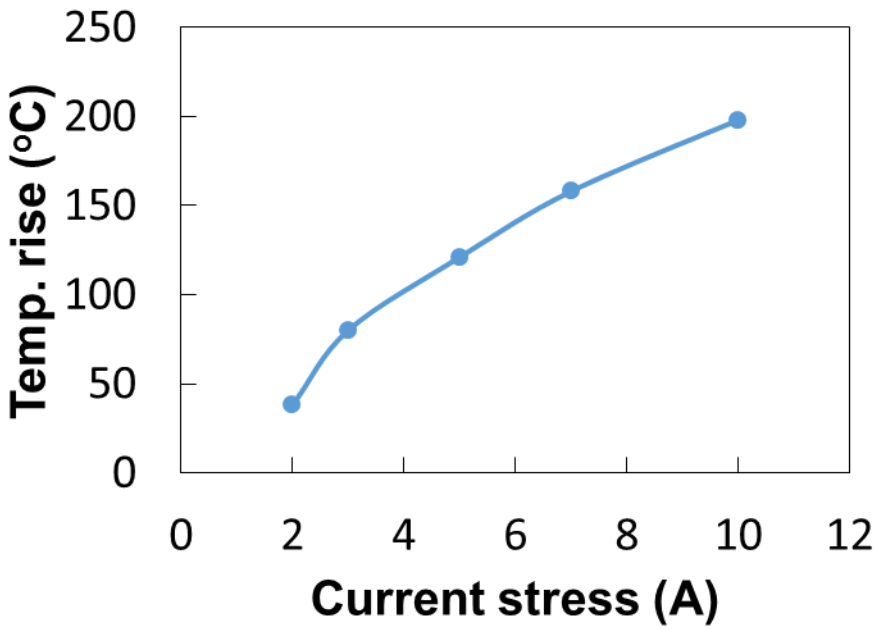

Figure 3.3. Temperature rise of the sample as a function of current stress.

3.2.2. Sample characterization

The sheet resistance of the deposited films were measured by four point probe technique. The structural properties of the MLG films were analyzed by Raman spectroscopy using an exciting laser of 532 nm wavelength and X-ray diffraction (XRD) analysis using Cu K_α radiation. The surface of the films was observed by scanning electron microscopy (SEM). The structures of the films were also analyzed by cross-sectional transmission electron microscopy (TEM).

3.3. Results and Discussion

3.3.1. Effect of current on formation and crystallinity of MLG by SPP

To investigate the effect of current stress on the formation and crystallinity of MLG films, firstly the annealing was carried out by setting the furnace temperature at 600 ^oC and current stresses of 2, 3, 5, 7, and 10 A were applied. Five samples were prepared. Secondly, we set the temperature of the furnace to the final temperature of the sample of the previous experiment including Joule heating and prepared 5 samples without current stress. Figures 3.4(a) and 3.4(b) show the comparison of Raman spectra between MLG films annealed at the same temperature without current and those annealed with current before Co removal. For example, we can see in Fig. 3.4(b) for the Raman spectrum for annealing at 600 ^oC with 3 A current that the measured sample temperature was 680 ^oC due to Joule heating. A similar position in Fig. 3.4(a) corresponds to the Raman spectrum for annealing at 680 ^oC without current. Therefore, in both cases, the sample temperature was 680 ^oC but (a) without and (b) with current. By comparing the two Raman spectra, we can investigate the effect of 3 A current at 680 ^oC. From the Raman spectra shown in Fig. 3.4, we can see that each spectrum is characterized by G, D, and 2D peaks. The G band is derived from the graphitic structure and the D band appears from disordered structures such as edges and grain boundaries [29]. MLG crystallinity is determined from G/D ratio. A higher G/D ratio leads to a higher crystallinity. The G/D ratio at 680 ^oC with 3 A current was higher than that at the same temperature without current. The maximum G/D ratio with current stress was approximately 8. The intensities of the G peaks of the MLG films annealed with over 5 A current were lower than those of the films annealed with 3 A current. The reason for the smaller G peaks is considered to be the smaller surface areas of the MLG films that determine Raman spectrum intensities as shown in Fig. 3.5 in next Sect. (SEM images of the sample surfaces after annealing with current stress), with the black area corresponding to the MLG decreased at over 5 A current compared with

that at 3 A current. For the samples with current stress as shown in Raman spectra of Fig. 3.4(b), there is an additional D′ peak. The splitting of the G peak into G and D′ peak occurs if there is an impurity associate with MLG. However, we have no supporting data with respect to impurity that limits the explanation of D′ peak in terms of impurity.

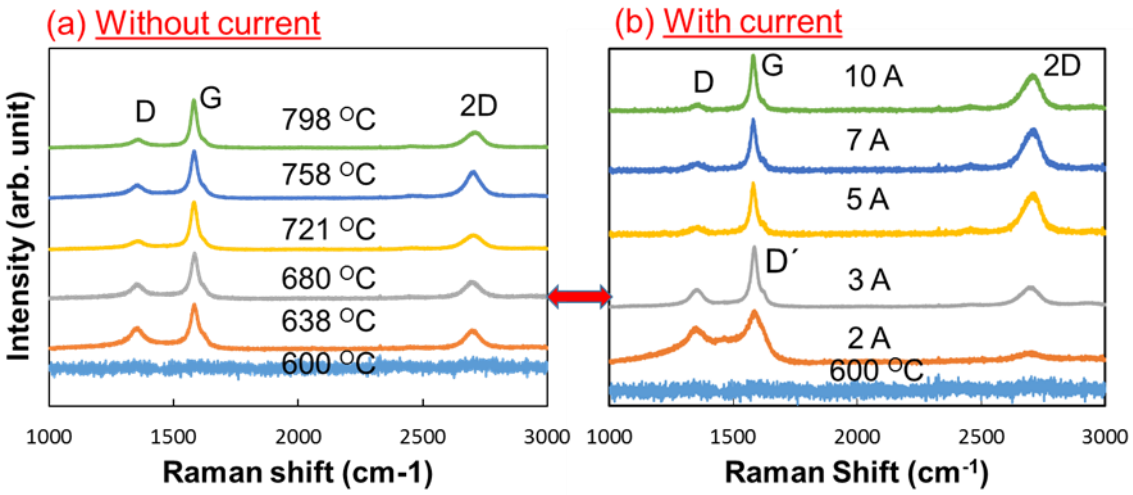

Figure. 3.4. Comparison of Raman spectra of MLG films annealed at different temperatures (a) without and (b) with current before Co removal.

Figure 3.5 shows the comparison of surface photograph measured by SEM of the Co-C layer after annealed at 680, 721, 758, and 798 ^{o}C (a) without and (b) with current stress varies between 3 and 10 A dc. From the SEM images shown in Fig. 3.5 one can observe different contrast on the sample surface. The reason behind the contrast difference might be due to the fact that the MLG formation is not uniform over the entire surface of the sample.

To confirm about the SEM image composition, we have measured the G/D and and G/2D Raman mapping on the sample surface within 1 µm x 1 µm area with 0.1 µm x 0.1 µm unit. Figures. 3.6 shows the (a) G/D and the (b) G/2D mapping of the sample surface annealed at 680 ^{o}C with 3 A current stress. The G/D ratio measures the crystallinity of the MLG film on the other hand the G/2D ratio measures the thickness of the MLG film. From the Raman mapping shown in Figs. 3.6, one can observe that, the position of the higher G/2D ratio in Fig. 3.6(b) corresponds to the higher G/D, i.e., the thick areas corresponds to MLG whereas, the thin areas corresponds to mostly Co.

Figure 3.7 shows the comparison of G/D ratios between MLG films annealed at the same temperature with and without current. It is seen from Fig. 3.7 that the G/D ratio increases with increasing current. The G/D ratio without current increases with temperature and then

decreases after reaching the peak. As the annealing temperature increases, more energy for graphitization is considered to be supplied, which leads to a higher G/D ratio. The G/D ratio

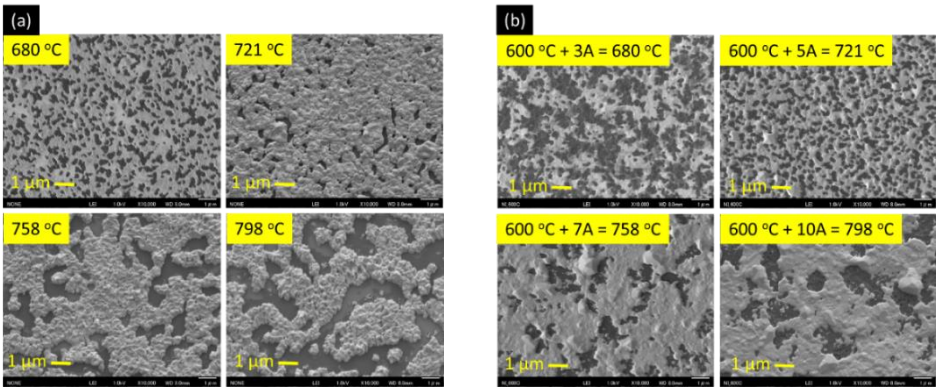

Figure 3.5. Comparison of surface photograph measured by SEM of the Co-C layer after annealed at 680, 721, 758, and 798 ºC (a) without and (b) with current stress

(a) (b)

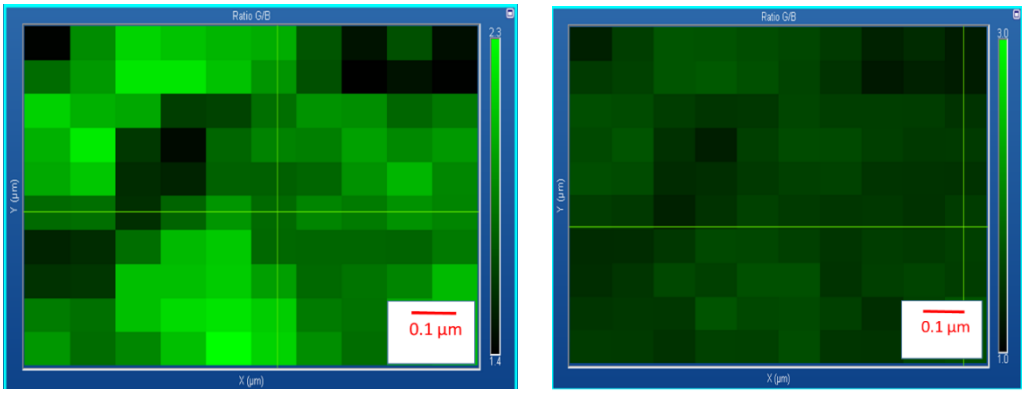

Figure 3.6. (a) G/D and the (b) G/2D mapping of the sample surface annealed at 680 ºC with 3 A current stress.

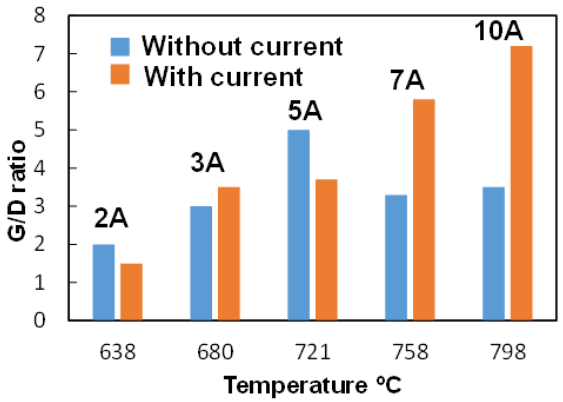

Figure 3.7. Comparison of G/D ratios of MLG films annealed at the same temperature without and with current.

increased with temperature up to 721 ^{o}C after which it decreased. Above the temperature of 758 ^{o}C, the G/D ratio of the films annealed with current stress was higher than that of the films annealed without current stress. Since annealing was conducted at the same temperature, the increase in the G/D ratio of the films annealed with current stress indicates that the effect of current stress was not only Joule heating but also the increase in G/D ratio as well as the crystallinity of MLG films.

3.3.2. Comparison of MLG crystallinity at the same temperature with different current stress

The results and discussion described in the previous Sect. are based upon the comparison of MLG crystallinity with and without current. We have changed the temperature as well as the current stress at the same time as described and showed in Table I in the previous Sect. To investigate the effect of current stress on formation and crystallinity of MLG more clearly by SPR, in this section we ought to describe the effect of current at a fixed temperature 680 ^{o}C but with changing the current stress between 3 and 10 A dc. To do so, we have measured the temperature property of the furnace again. In this case, we set the furnace at different temperatures such that applying current stress leads to the same temperature of the sample that is 680 ^{o}C, as summarized in Table II.

Table 3.2. Set temperatures of the furnace and applied current to obtain constant sample temperature.

Set temperature with dc stress	Temperature of sample
580 ^{o}C + 3 A	680 ^{o}C
490 ^{o}C + 6 A	680 ^{o}C
467 ^{o}C + 8 A	680 ^{o}C
380 ^{o}C + 10 A	680 ^{o}C

Figure 3.8 shows the comparison of Raman spectra between MLG films annealed at the same temperature of 680 ^{o}C without and with various current stresses. From Raman spectra, it was found that annealing at the same temperature but higher current stresses leads to an

increase in the G/D ratio. Figure 3.9 shows the point-by-point variations of G/D ratios within the samples of MLG films annealed at the same temperature with different current stresses (a) before and (b) after Co removal. In both cases, we can see that the G/D ratio tends to increase with current stress at the same temperature annealing. Thus, MLG fabrication by applying

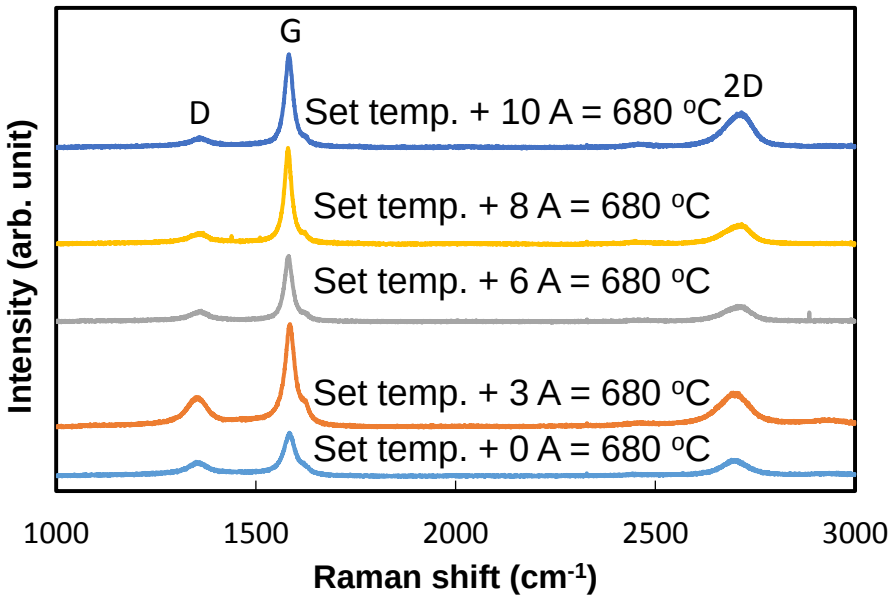

Figure 3.8. Raman spectra of MLG films annealed at 680 ºC without and with various current stresses.

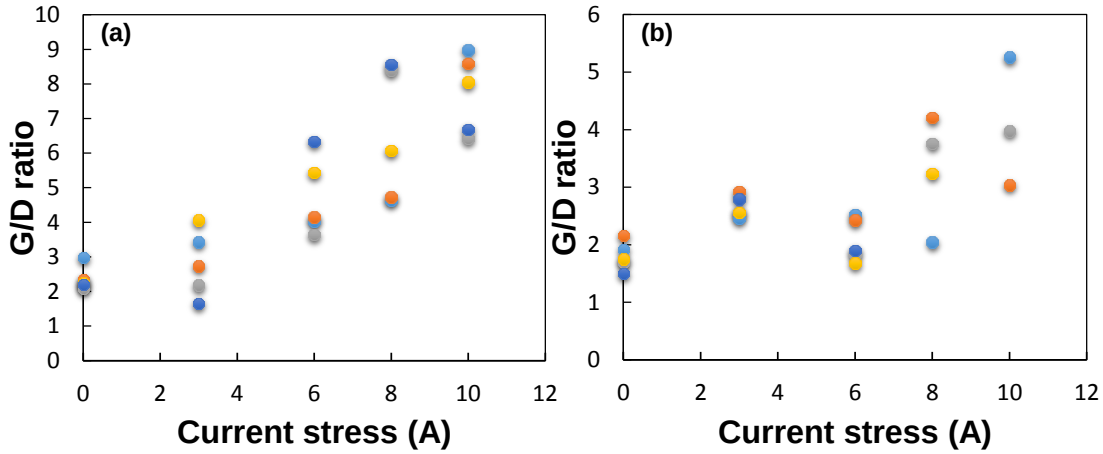

Figure 3.9. Point-by-point variation of G/D ratios of MLG films annealed at 680 ºC without and with various current stresses (a) before and (b) after Co removal.

current stress during annealing showed improved crystallinity in comparison of those annealed without current stress at the same temperature annealing.

MLG grain size can be calculated by using the G/D ratio from Raman spectra [30]. The equation for determining the MLG grain size can be written as follows

$$L_a(nm) = (2.4 \times 10^{-10})\lambda_l^4 \left(\frac{I_D}{I_G}\right)^{-1} \quad (3.1)$$

Where L_a is the MLG grain size, λ_l is the wavelength of the excitation laser used in raman measurement and I_D and I_G belongs to the area intensity of the D and G peak.

Using Eq. 1 and the the D and G peak intensity from the raman spectra shown in Fig. 3.8 one can calculate the MLG grain size. Figure 3.10 shows the variation of MLG grain size with current stress before and after Co removal. From Fig. 3.10, it is clearly seen that the MLG grain size increases with increasing current stress at the same temperature of 680 ^oC even after Co removal.

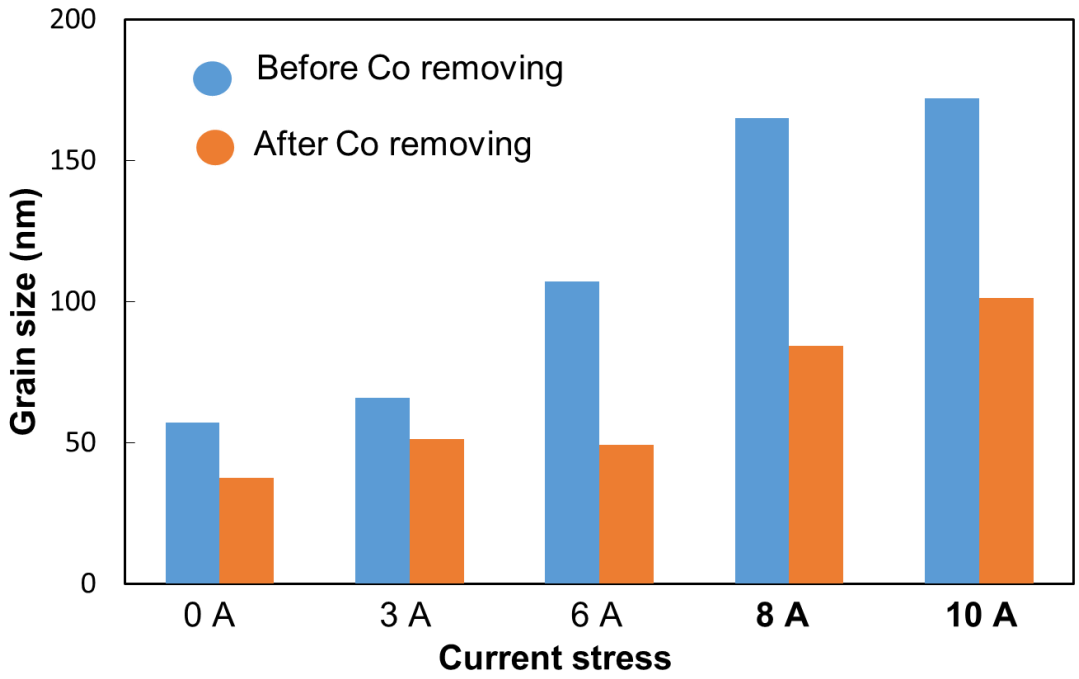

Figure 3.10. Variation of MLG grain size with current stress at 680 ^oC before and after Co removal.

Figure 3.11 shows the SEM photographs of the surface of the MLG films annealed at 680 ^oC (a) without, (b) 6, (c) 8, and (d) 10 A dc. All the SEM photographs show the non-uniform growth of MLG over the substrate. From the SEM photographs, one can observe the increase in the MLG grain size of the film annealed with applied current compared with that of the film annealed at the same temperature without current. From the Raman spectroscopy and SEM photographs, we found the increase in the grain size of the film annealed with applied current at the same temperature. The reason for the increase in MLG grain size might be as follows. When no current is applied during annealing at the same temperature, the nucleation

of MLG occurs at many sites as shown in the SEM photograph in Fig. 3.11(a) and we can see many grains. As shown in Fig. 3.11(b) to (d), annealing at the same temperature with current stress led to a decrease in the number of grains, resulting in the increase in grain size. This

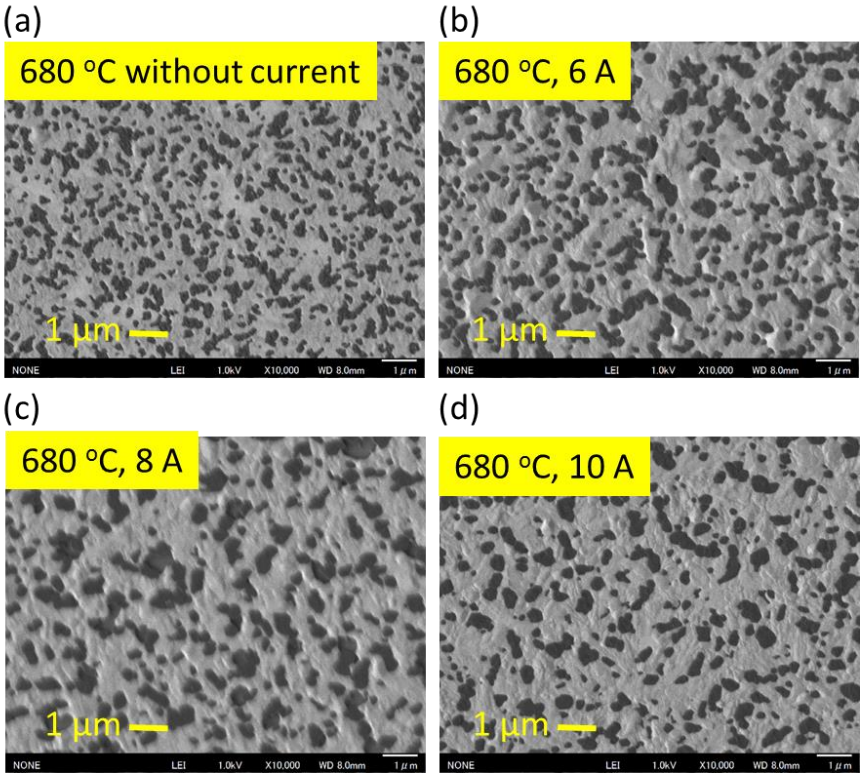

Fig. 3.11. SEM images of the surface of the annealed films annealed at 680 ^{o}C (a) without, (b) 6, (c) 8, and (d) 10 A dc

means that the current stress during annealing may be responsible for (a) nucleation to occur at some particular sites due to the fact that the crystallization of the Co catalyst may be enhanced by agglomeration (will be shown in XRD spectra later). The enhancement of Co-crystallization by current stress may be caused by enhancing C-diffusion in Co that leads to agglomeration of Co. As a result of Co-agglomeration the nucleation sites of MLG decreased. The reduction in the number of nucleation sites of MLG by current stress, the number of MLG grains decreased and MLG grain size increased. It is reported that current stress during thermal CVD can improve MLG crystallinity significantly [26, 27]. The results shown here are in accordance with the reported results regarding the effect of current during thermal CVD of MLG. Therefore, current stress is considered a potential method to improve the crystallinity of MLG in both SPR and thermal CVD.

As shown in Figs. 3.9 and 3.10, the G/D ratio as well as the MLG grain size decreased after Co removal. The MLG grains may be grown over the Co grains, and removing the Co

layer may lead to the decrease in MLG grain size as well as G/D ratio. This might be due to the MLG growth that occurred at the bottom of the Co layer as well as on the Co layer, as shown in the SEM and TEM photographs in next Sect.

Figure 3.12 shows a cross-sectional TEM image of a MLG film annealed at 680 ^{o}C with 6 A current applied. From the TEM image, we can see that graphene layer structures exist on the substrate. The presence of these structures confirms the formation of MLG. From Fig. 10, we can see MLG layers existing under the Co layer as well as on the Co layer. This means that the growth of MLG took place at the sides of the Co layer. When the sputtered film was annealed at a high temperature, the Co catalyst agglomerated and islands were formed between the agglomerated portions of the Co layer. Yamazaki et al. [31] studied low-temperature graphene growth originating from crystalline facets of a catalytic metal and reported the graphene growth on Ni/Co catalysts originating from crystalline facets by plasma-based CVD. In our experiment, MLG growth took place from the facet as shown in Fig. 3.12.

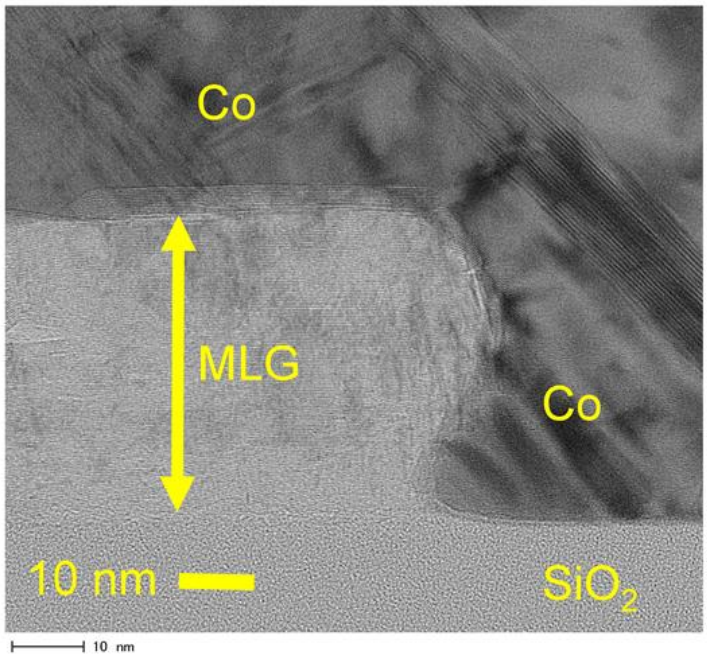

Figure 3.12. Cross-sectional TEM image of the MLG film annealed at 680 ^{o}C with 6 A dc applied.

Figure 3.13 shows the XRD profile of Co-C films annealed at 680 ^{o}C without and with 6, 8, and 10 A current applied. As shown in Fig. 11, the graphite (0002) peak with various Co peaks is observed under each annealing conditions. The existence of this graphite (0002) peak confirms the formation of MLG. It can be seen that the intensity of both graphite (0002) and graohite (004) peaks increased significantly after applying current stress in comparison with that without current. The higher graphite peaks after applying current during annealing

indicates the improvement of MLG crystallinity. The hcp Co(1011) peak near 42^{o} exists before current application, but when current was applied during annealing, the hcp Co(1011) peak disappears. From the XRD profile shown in Fig. 3.13, we can see that the intensities of fcc

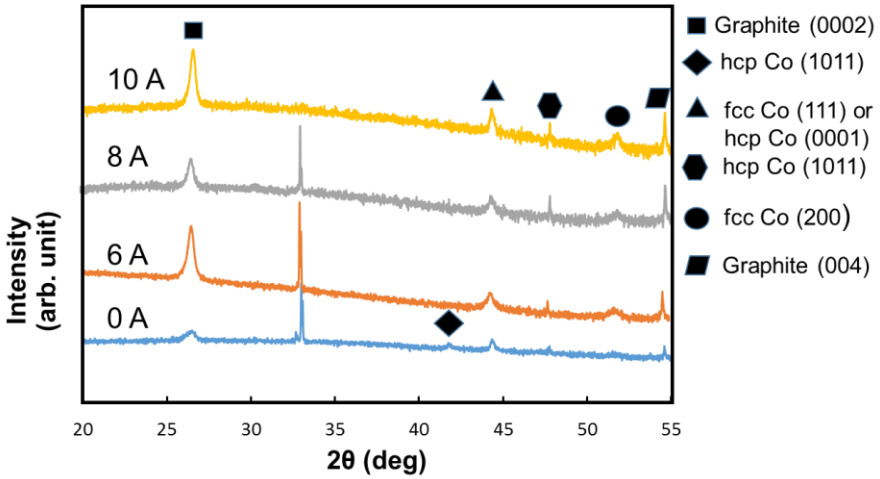

Figure 3.13. XRD profile of the sample annealed at 680 ^{o}C without and with 6, 8, and 10 A dc applied.

Co(200) peak increased sharply after current was applied. The Co peak close to 44^{o} shows two stable phases are fcc Co(111) or hcp Co(200). The hcp phase is stable upto 412 ^{o}C and the fcc phase is stable above this temperature [21-23]. We have annealed the Co-C layer at various temperatures ranging from 600-798 ^{o}C. This is why the fcc phase become stable. The observed peak near 44^{o} is the fcc Co(111) or hcp Co(0001) as in this case both fcc and hcp phases co-exist. Saadi et al. [32], theoretically studied the adsorption energies of carbon atoms on Co surfaces during graphene growth. Since the atomic arrangements of fcc (111) and hcp (0002) are the same, the adsorption energies for both surfaces are the same at 1.20 eV as reported by Saadi et al. However, the adsorption energy of carbon was found to be 0.42 eV in the case of the fcc step, which is smaller than that in the case of the hcp or fcc terrace. Owing to the formation of new fcc phases of Co after applying current stress at the same temperature, it is easier for carbon atoms to form MLG at the fcc step site. Therefore, the predominance of fcc Co after applying current stress may be another reason for the improvement of MLG crystallinity.

Figure 3.14 shows the XRD spectra comparison between MLG films deposited at 680 ^{o}C by application of 6 A current before and after Co removal. From the XRD spectra shown in Fig. 3.14, one can observe the existence of Co (111) as well as Co (200) peaks. Both the Co peak vanishes when the XRD measurement was taken for the same sample after Co removal, i.e, the Co was removed from the MLG surface properly. Another noticeable point is that, the

graphite peaks both (002) and (004) were seen to be unaffected after Co removal. That means, our Co removal procedure was only effective in removal of the Co from the substrate with the MLG layer unaffected.

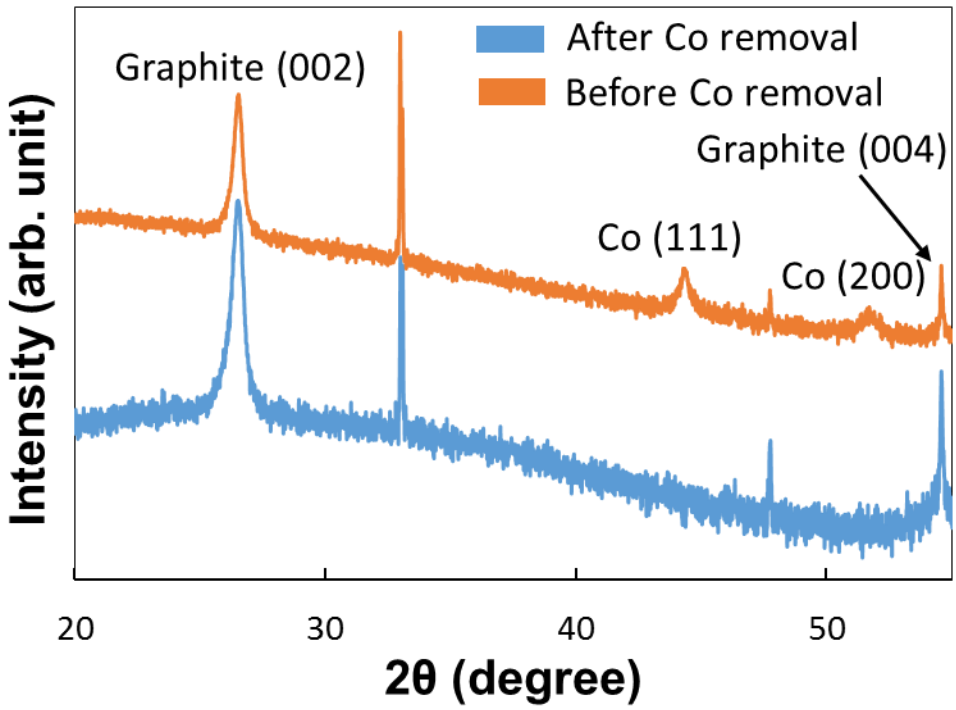

Figure 3.14. XRD spectra comparison between MLG films deposited at 680 ^{o}C by application of 6 A current before and after Co removal.

3.3.3. Improvement of MLG uniformity

From the SEM and TEM photographs shown in the previous Sects. we found that the formation of MLG was not uniform over the entire surface of the substrate. To apply MLG in narrow interconnects, the uniformity of MLG in thickness and sheet resistance is necessary. The uniformity of MLG can be improved by depositing an additional Cu capping layer over the Co-C layer [28], which is already demonstrated.

The experimental process flow for the fabrication of uniform MLG on SiO_2 by SPR is shown in Fig. 3.15. The SiO_2 substrates were cleaned with exactly identical procedure of the previous experiment. After that Co-C layer of thickness 100 nm and Cu as a capping layer of thickness 50 nm were deposited onto the SiO_2 substrate by magnetron sputtering. Annealing of the sputtered structures were carried out in vacuum of 5 x 10^{-3} Pa at 680 ^{o}C without current

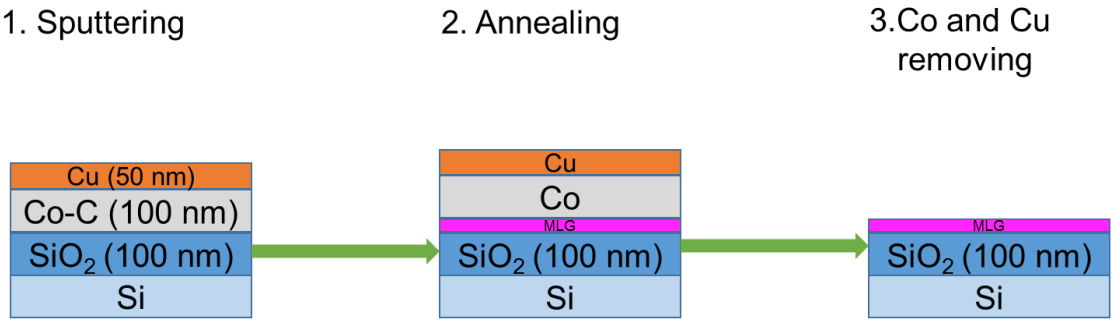

Figure 3.15. Process flow for the fabrication of uniform MLG on SiO_2 substrate with additional Cu capping layer.

stress and with various current stress between 3 to 10 A dc. During annealing and cooling C should precipitates only below the Co layer. The Cu capping layer on the Co layer should oppose the C atoms to precipitates above the Co layer. Since Cu does not make alloy with Co at the annealing temperature (680 ^{o}C) [33], used during our experiment. The Cu-Co phase diagram is shown in Fig. 3.16. The Co and the Cu layers were removed from the upper surface of the MLG layer by H_2SO_4 and H_2O_2 solutions.

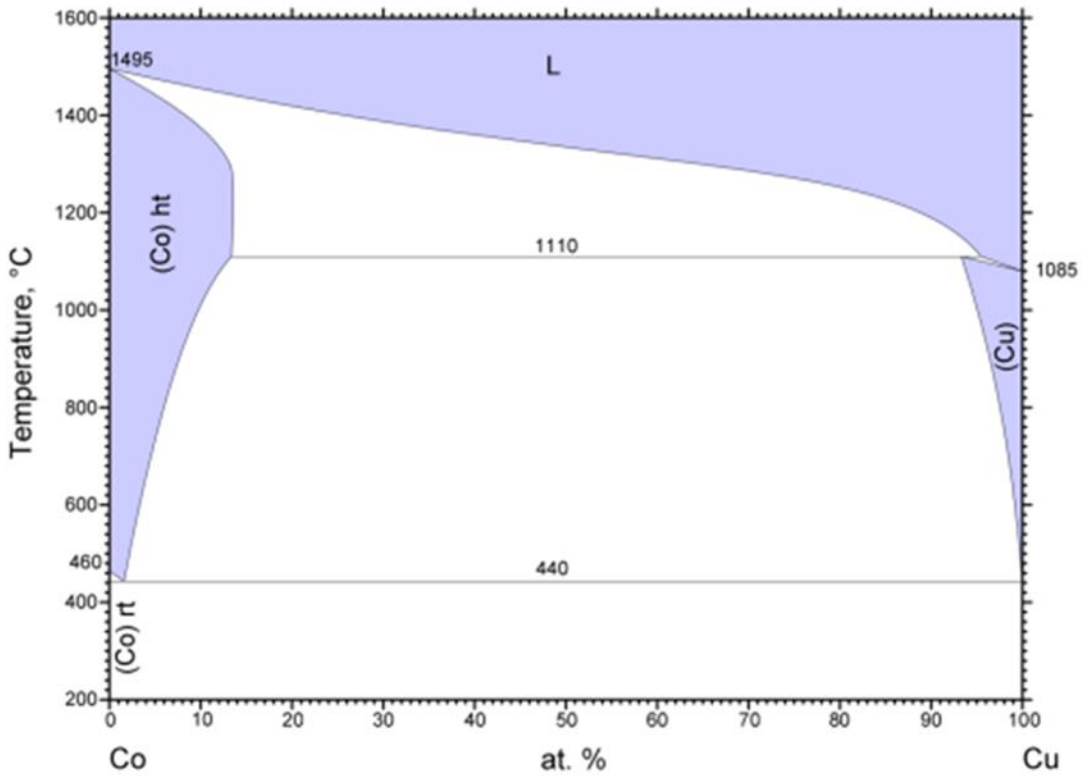

Figure 3.16. The Co-Cu phase diagram, image [33].

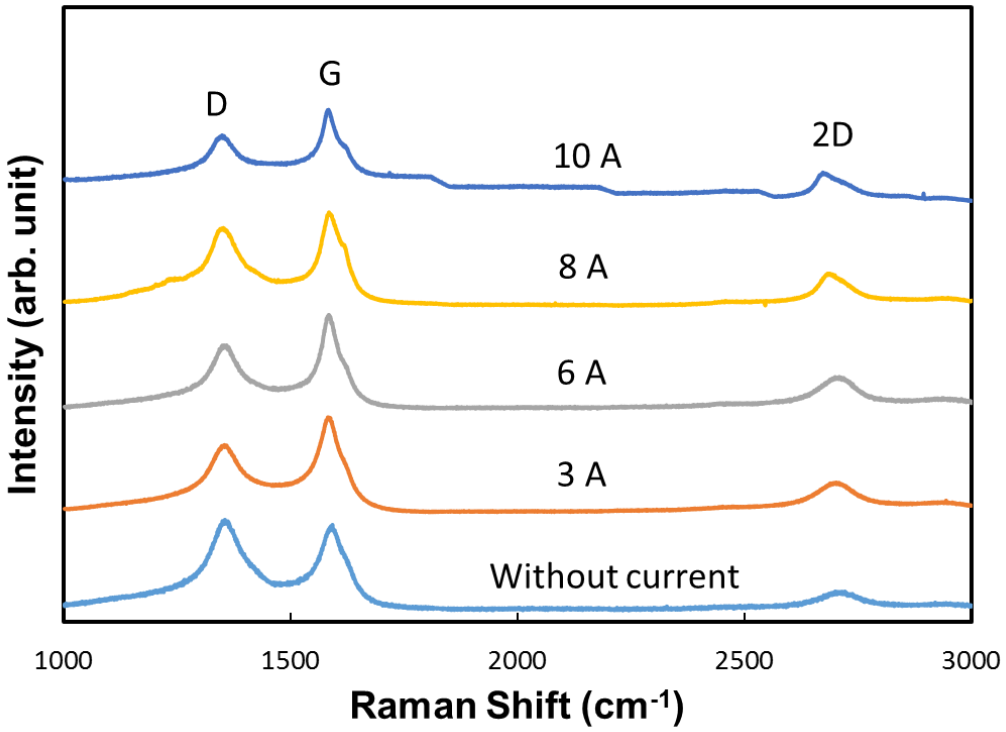

Figure 3.17. Comparison of Raman spectra among MLG films deposited by annealing Co-C layer with a Cu capping layer at 680 ^{o}C without current and with various currents.

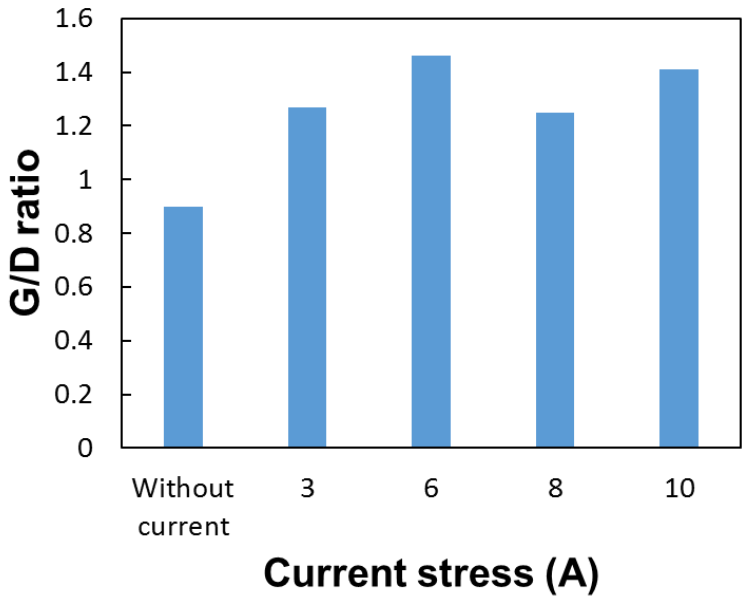

Figure 3.18. The variation of G/D ratio of MLG films after annealing of Cu/Co-C layer at 680 ^{o}C without current and with current stress varies between 3 to 10 A dc.

Figure 3.17 shows the comparison of Raman spectra among MLG films deposited by annealing Co-C layer with a Cu capping layer at 680 ^{o}C without current and with various currents between 3 and 10 A dc. From the Raman spectra, it is seen that the graphitization occurred at each annealing conditions as the spectra are characterized by distinct D, G, and 2D peaks. For the samples with current stress application the G peak intensities are seen to be greater than D peak intensity. Figure 3.18 shows the comparison of G/D ratios between MLG films deposited at 680 ^{o}C without current and with various current with a 50 nm Cu capping layer on Co-C layer. It can be seen from Fig.3.17 that the G/D ratio for the MLG films with current stress was larger than the sample without current. Thus, current stress can improve the MLG crystallinity even if the Cu capping layer was used on the sputtered Co-C layer.

Figure 3.19 shows the SEM photographs of the MLG films deposited at 680 ^{o}C with current stress varies between 3 to 10 A dc (a) without and (b) with 50 nm Cu capping layer. From Fig. 3.18, we can see that, by depositing an additional Cu capping layer over the Co-C layer, the uniformity of the MLG layer is improved significantly. When a Cu capping layer is deposited over the Co-C layer, the Cu layer can suppress the agglomeration of Co, which leads to the uniform precipitation of MLG, since Cu does not form an alloy with Co at the annealing temperature 680 ^{o}C as we have mentioned already. Therefore, adding a Cu layer over the Co-C layer as the capping layer leads to the improvement of the uniformity of MLG films fabricated by SPP, although further optimization is necessary for the improvement of G/D ratio.

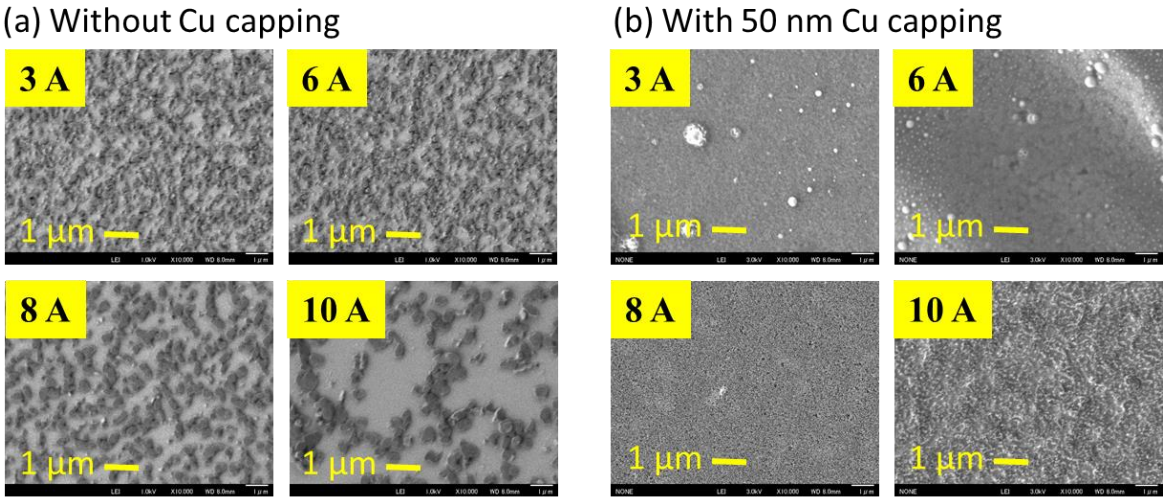

Figure 3.19. SEM photographs of the MLG films deposited at 680 ^{o}C with current stress varies between 3 to 10 A dc (a) without and (b) with 50 nm Cu capping layer.

3.4. Summary and conclusions

For the application of MLG as an interconnect material, it requires transfer-free MLG films with higher crystallinity and uniformity deposited at lower temperature. To fabricate MLG films with improved crystallinity by SPR, a new technique of current stress application during annealing of Co-C layer was demonstrated for the first time. To improve the uniformity of MLG films, a Cu layer at the top of the Co-C layer was used. The results of the current chapter can be summarized as follows

- MLG was fabricated directly on SiO_2 substrates by SPR with current stress application during annealing of a Co-C layer at a comparatively lower temperature for the first time.
- The effects of current stress on the formation and crystallinity of MLG films were investigated by comparing the characteristics of the films annealed at the same temperature with and without current by taking into account the temperature rise due to Joule heating.
- The characteristics obtained by Raman spectroscopy, scanning electron microscopy (SEM), transmission electron microscopy (TEM), and X-ray diffraction (XRD) measurements revealed that the MLG films produced were crystalline in nature and the crystallinity of the MLG films with current stress was better than those without current at the same temperature. The crystallinity of MLG films with current stress was found to be increased with applied current stress at the same temperature.
- From SEM and XRD measurements, beside Joule heating, enhancement of Co grain size by agglomeration induced by current stress may be the potential reason for the improvement of the crystallinity of MLG films.
- MLG growth was found to be originated from crystalline facets as was confirmed by the cross-sectional TEM measurement.
- From XRD measurement, fcc Co phase were found to be predominant by applying current stress in comparison with those without current annealing at the same temperature. The dominancy of fcc Co might be another reason behind improvement of crystallinity.
- Uniformity of MLG films were improved the by depositing an additional copper (Cu) capping layer over the Co-C layer. Since Cu does not make alloy with Co at the temperature used for annealing during experiment, the agglomeration of cobalt was stopped by Cu as a capping layer.

Finally, it may be concluded that MLG fabrication by SPR with current stress application during annealing can lead to low temperature fabrication of MLG with higher crystallinity and uniformity in comparison with conventional annealing. The low temperature MLG deposition with improved crystallinity and uniformity by our new method might be potential for the application of MLG as an interconnect with further improvement.

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CHAPTER FOUR
CATALYST-FREE DEPOSITION OF NANOCARBON ON n-GaN BY SOLID-PHASE REACTION

4.1. Overview

In previous chapter, we have deposited transfer-free multilayer graphene (MLG) on SiO_2 with improved crystallinity and uniformity by solid-phase reaction (SPR). In this chapter we will study on fabrication of MLG on n-GaN by SPR.

4.2. Background and Objectives

Gallium nitride (GaN) is a direct bandgap semiconductor belonging to the III-V group. The compound is very hard, and has a Wurtzite crystal structure. It has a wide band gap of 3.4 eV enabling it to be used in optoelectronic, high-frequency and high-power applications. The devices fabricated in these material systems include light emitting diodes (LEDs) [1], lasers [2], metal-semiconductor-metal [MSM] photodetectors [3], hetero junction filed effect transistors (HFETs) [4], high-electron-mobility transistors (HEMTs) [5], metal oxide semiconductor field effect transistor (MOSFETs) [6], and Schottky rectifiers [7]. The performances of these devices can be influenced by Schottky barrier height (SBH), the reverse leakage current, and the thermal stability of the Schottky contact. Schottky contacts to n-type GaN with various metal schemes have been investigated by several groups e.g., Ni [8], TaN [9], Pt [10], Au [11], W_2B_5 [12], ZrB_2 [13], and Mo [14]. C. Y. Wang et.al. [8], investigated the thermal annealing effects on electrical and structural properties of Au/Ni/n-GaN Schottky diodes. In their study, the diodes performance degrades and the diodes become non-rectifying after being annealed at temperatures higher than 500 ^oC. Order et.al [11], studied the electrical properties and thermal stability of ZrB_2 Schttky contact to n-GaN and reported that the barrier height decreased after annealing at 300 and 400 ^oC. K. J. Reddy et al [15], studied on the thermal annealing behavior on Schottky barrier parameters and structural properties of Au contacts to n-type GaN and reported the degradation of barrier height after annealing at 500 ^oC. They summarized the formation of Au gallide phases as the reason behind degradation of the barrier height. The performance of GaN based device are limited to several materials and engineering problems, including the difficulty of making reliable metal contacts [16]. Therefore, it is necessary to develop of more reliable and thermally stable Schottky contact for

the application of power amplifiers and opto-electronic devices operating at higher temperatures.

Graphene or multilayer graphene (MLG) is expected as an alternative Schottky metal on n-GaN owing to its outstanding physical and optical characteristics such as high intrinsic electron mobility, quantum electronic transport, low optical absorption, and good chemical and mechanical stabilities [17-21], and its high barrier height, low reverse leakage current, and high thermal stability have been reported [22,23]. Graphene has been synthesized by various methods, among which chemical vapor deposition (CVD) on a metal substrate is the most common method for obtaining large-area high-quality graphene films [24-30]. However, for most of the device fabrication methods, graphene synthesized on a metal substrate requires an additional transfer step, which may not be ideal for many applications. In this context, synthesis of transfer-free graphene/MLG directly on n-GaN can be a promising approach for obtaining the most interesting physical and electrical properties of graphene/MLG for device applications [31-35].

Very recently, a number of studies focusing on the fabrication of transfer-free MLG on n-GaN substrates by chemical vapor deposition have been reported by several groups [36, 37]. Z. Yuan et al [36], studied on the direct growth of graphene on GaN by using chemical vapor deposition without extra catalyst. They reported the formation of 5-6 layer of graphene films by using CH_4 as the precursor gas for the formation of the graphene film. They have optimized the CVD temperature to be 950 ^oC. B. Wang et al [37], studied on the catalyst free deposition of graphene films by thermal CVD with C_2H_2 as the carbon source for CVD. They have reported that the fabrication temperature can be reduced to 830 ^oC by using C_2H_2 as carrier gas in place of CH_4. However, both of the groups [36,37] reported the formation of MLG took place without any effect of GaN epi-layers. J.Sun et al. [38] studied on direct chemical vapor deposition of large area carbon films on GaN. They have reported that catalyst free deposition of thin carbon film is possible by thermal CVD at 950 ^oC. They fabricate carbon thin film with distinct D and G peak but no 2D peak was observed.

The formation mechanism of MLG on n-GaN by catalyst-free CVD as reported in Refs. 36 and 37 can be explained as follows. When the precursor flows through the furnace at high temperatures, GaN chemically react with precursor and seperates the Ga atoms and the N_2 reacts with H_2 to make NH_3 and exusted as byproduct gas. The Ga atoms are then acts as catalyst for the transformation of a-C to graphene. In this context, we expect the formation of MLG by SPR under high temperature annealing of sputtered a-C layer on n-GaN layer. At high

temperatures, GaN is expected to be breaks up by Ga and N_2 and the Ga atoms are expected to be acted as catalyst for the formation of MLG.

4.3. Experimental methods

4.3.1. Sample preparation

The process flow of MLG fabrication is shown in Fig. 4.1. As the substrate, commercially available n-GaN layer purchased from POWDEC of 1 µm thickness on 2 µm undoped GaN (u-GaN) grown on sapphire was used. The dopant for n-GaN was Si and the carrier concentration (n) was from 6 x 10^{16} to 1 x 10^{17} cm^{-3}. A buffer layer (GaN) separated u-GaN and sapphire. The thickness of the buffer layer was 30 nm. The n-GaN substrates were cleaned ultrasonically with

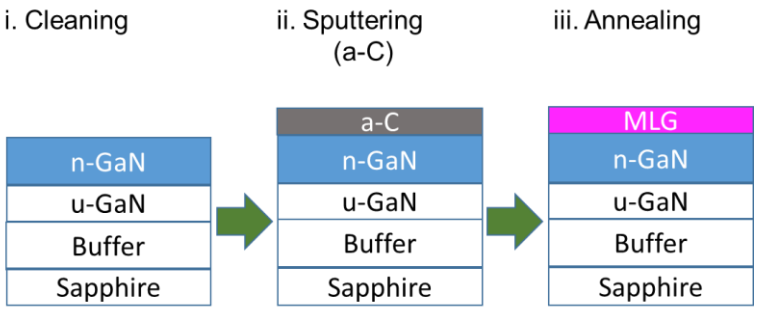

Figure 4.1. Process flow of fabrication of MLG on n-GaN without extra catalyst by solid-phase reaction.

tetramethylammonium hydroxide (TMAH), isopropyl alcohol (IPA), and ultrapure water. The substrates were then dipped in concentrated HCl to remove the native oxide layers and then again cleaned in ultrapure water ultrasonically and finally dried in nitrogen flow. An amorphous C layer of 15 nm thickness was deposited on n-GaN by magnetron sputtering. The flow rate of Ar was 20 sccm and the pressure was 1 Pa with a base pressure of 7.0×10^{-4} Pa. The sputtering powers for C was 400 W. The structure of the sputtered film was a-C/n-GaN (upper layer/lower layer). The sputtered structures were then annealed in a tube furnace at various temperatures between 800 and 1000 ^{o}C at intervals of 100 ^{o}C. The annealing time was 30 min in a vacuum of 5×10^{-3} Pa.

4.3.2. Sample Characterization

The structural properties of the annealed films were analyzed by Raman spectroscopy using an excitation laser of 532 nm wavelength. X-ray diffraction (XRD) analysis using Cu Kα radiation

was carried out to analyze the crystal structures of annealed a-C/n-GaN. The surface of the films was observed by scanning electron microscopy (SEM) and optical microscopy.

4.4. Results and discussion

Figure 4.2 shows the Raman spectra of sputtered a-C/n-GaN films before annealing and after annealed at various temperatures between 800 and 1000 ^{o}C. From the Raman spectra shown in Fig. 4.2, one can observe the formation of nano-carbon based materials as the spectra for annealed structure is characterized by distinct G and D peaks. The nanocarbon material are not MLG as there is no distinct 2D peaks. The property of the fabricated nanocarbon is similar to diamond like carbon (DLC). The formation of NC materials might be due to the fact that upon

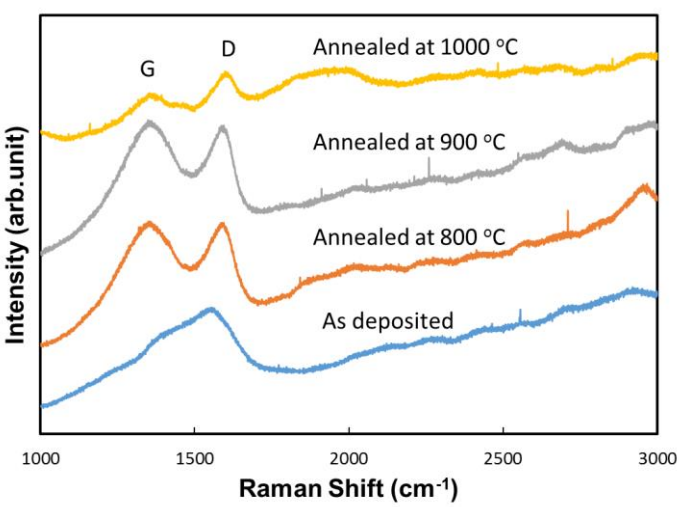

Figure 4.2. Raman spectra of sputtered a-C/n-GaN films without annealing and after annealed at various temperatures.

annealing at a high temperature and cooling down to room temperature, a fraction of a-C atoms might be crystallized in diamond lattice. Thus the annealed structure might be the combination of a-C and diamond crystallites.

Figure 4.3 shows the optical microscopy of the surface of the a-C/n-GaN films annealed at (a) 800, (b) 900, and (c) 1000 ^{o}C. From the surface photographs shown in Figs. 4.3, it is seen that the surface of the film for annealing at 800 ^{o}C is very rough. The surface roughness decreasing with the increase of annealing temperature. Annealing at 1000 ^{o}C the sample surface became smoother. The reason behind the the surface improvement might be due to the fact that the surface contaminants might be cleaned after the annealing temperature is increased.

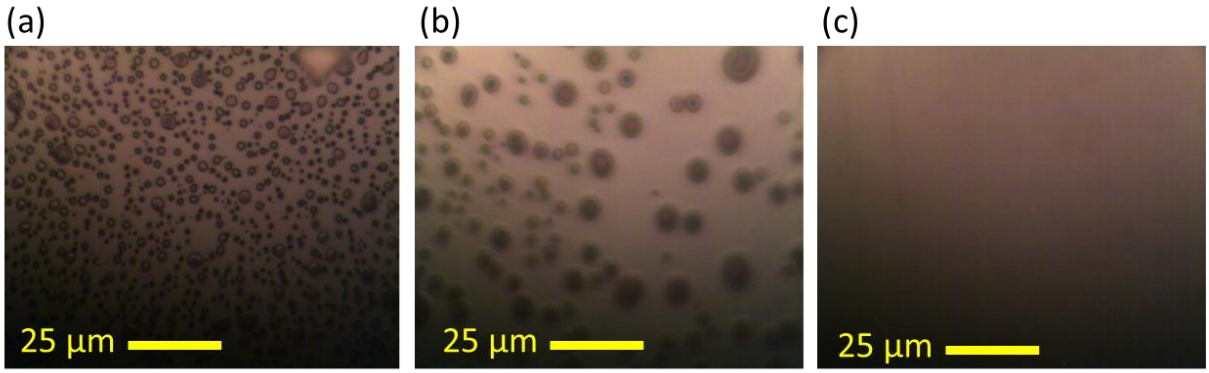

Figure 4.3. Surface images taken by optical microscopy of the sputtered a-C/n-GaN layer after annealed at (a) 800, (b) 900, and (c) 1000 ^{o}C.

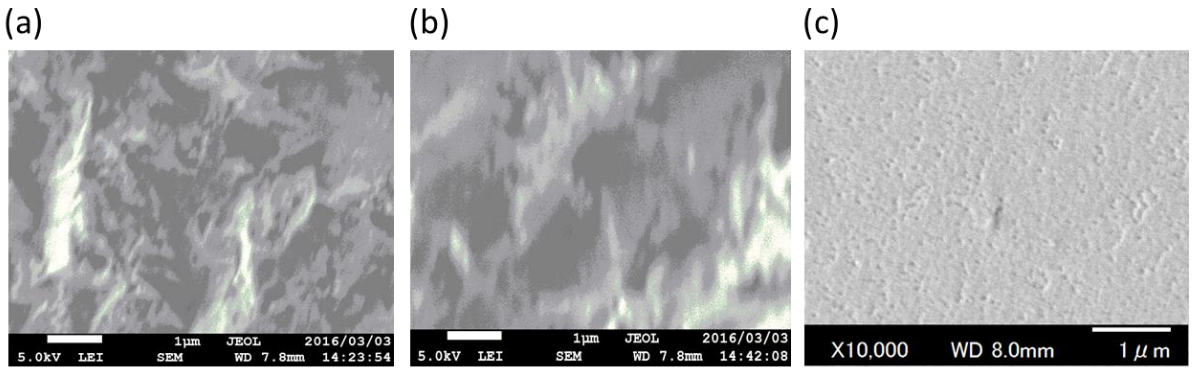

Figure 4.4. Surface images taken by SEM of the sputtered a-C/n-GaN after annealed at (a) 800, (b) 900, and (c) 1000 ^{o}C.

Figure 4.4 shows the surface SEM images of the a-C/n-GaN films annealed at (a) 800, (b) 900, and (c) 1000 ^{o}C. From the SEM images of Figs. 4.4 one can observe the surface roughness decreases with the increase of annealing temperature. Annealing at 1000 ^{o}C lead to the optimum surface condition.

Figure 4.5 shows the XRD spectra of sputtered a-C/n-GaN films without annealing and after annealed at 1000 ^{o}C. From the XRD spectra comparison of Fig. 4.5, we can see that a small Ga peak is observed after annealing of the a-C/n-GaN film at 1000 ^{o}C. The GaN may be broken up with Ga and N during the high temperature annealing of the sample. The N_2 might be evacuated by the vacuum pump that was engaged to evacuate the annealing chamber. The breaking of GaN into Ga and N_2 might be another reason behind the crystallization of the a-C

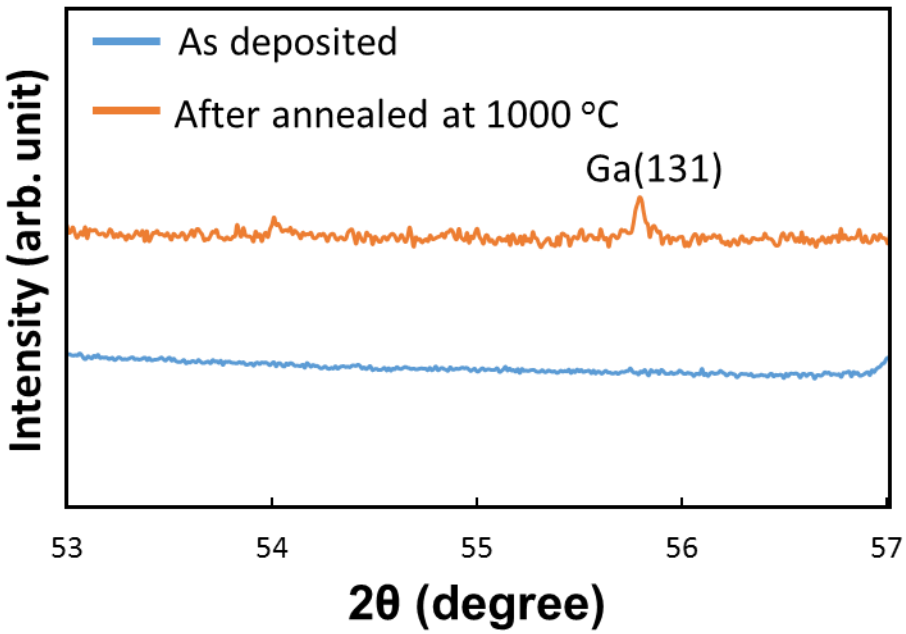

Figure 4.5. XRD spectra of sputtered a-C/n-GaN films before annealing and after annealing at 1000 ^{o}C.

Layer upon annealing. The escaped Ga atoms from GaN might be acted as a catalyst to solid-phase reaction to occur between Ga and a-C and upon cooling the structure to room temperature the a-C might be partially crystallize to form diamond like carbon. Another noticeable phenomenon is seen from the XRD spectra is the disappearance of some unknown peaks after annealing at 1000 ^{o}C. That means the unknown contaminants from the surface of the sample was cleaned due to high temperatures. This cleaning of the contaminants might be the reason behind the improved surface condition as was confirmed from the SEM images discussed in the previous sections.

4.5. Summary and Conclusions

For the fabrication of MLG based n-GaN device, it is preferable to deposit MLG on n-GaN directly which requires no transfer process. This chapter is the first attempt to fabricate transfer-free nano-carbon films on n-GaN by SPR by annealing sputtered a-C on n-GaN. The obtained results of the current chapter can be summarized as follows

- Diamond like carbon films were found to form by annealing the a-C layer on n-GaN at temperatures between 800 and 1000 ^{o}C as the Raman spectra were characterized by D and G peak with absence of 2D peak.
- The surface uniformity of the samples were seen to be increase with the increase of annealing temperature. Crystallization of a-C occurred due to high temperature

annealing or self-catalization of Ga by breaking of GaN into Ga and N_2 at high temperature as was seen from XRD spectra.

However, by this method the fabricated nanocarbon film is not MLG. To reach the our goal of fabricating a MLG based GaN device, transfer-free deposition of MLG with improved crystallinity and uniformity will be required. In addition, lowering of the deposition temperature is required to reduce C diffusion to GaN.

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CHAPTER FIVE

TRANSFER-FREE DEPOSITION OF MULTILAYER GRAPHENE WITH IMPROVED CRYSTALLINITY ON n-GaN BY SOLID-PHASE REACTION

5.1. Overview

From the results and discussion from the previous chapter, diamond like carbon (DLC) films were found to form by annealing sputtered amorphous carbon (a-C) on n-GaN. The deposition temperature was as high as 1000 ^{o}C and the crystallinity of the deposited film was not good. Our aim is to fabricate a multilayer graphene (MLG)/ n-GaN Schottky barrier diode (SBD). In this context, we want to focus on fabrication of MLG on n-GaN for the reflection of MLG/n – GaN Schottky barrier diode (SBD) properties. Also we need to reduce the deposition temperature to minimize the C diffusion to GaN. In this chapter, we will focus on transfer-free deposition of MLG on n-GaN with improved crystallinity at lower deposition temperature.

5.2 Background and Objectives

Nitride based semiconductor such as Gallium nitride (GaN) are being intensively studied for application in high temperature and high frequency operations including light emitting diodes (LEDs) [1], lasers [2], metal-semiconductor-metal [MSM] photodetectors [3], hetero junction filed effect transistors (HFETs) [4], high-electron-mobility transistors (HEMTs) [5], metal oxide semiconductor field effect transistor (MOSFETs) [6], and Schottky rectifiers [7]. As discussed in the previous chapter, a reliable and thermally stable Schottky contact is required for the application of n-GaN based device mentioned in Refs. 1 to 7. MLG can be used as a alternate Schottky metal owing to its outstanding properties. For the fabrication of a MLG based Schottky diode, it requires MLG on n-GaN. For most of the device fabrication, graphene/MLG grown on a metal substrate requires an additional transfer step. To reflect the most promising properties of MLG based n-GaN device, transfer-free deposition is better. Several research groups [8,10] reported on transfer-free deposition of MLG on n-GaN by thermal CVD. The reported deposition temperature was high and crystallinity was not good. We also attempted to fabricate MLG on n-GaN by solid-phase reaction (SPR) as reported in the previous chapter. But, the deposited film was not MLG but DLC and the deposition

temperature was as high as 1000 ^{o}C. The fabrication temperature should be decreased to suppress C diffusion through GaN [11].

In this chapter, the fabrication process of transfer-free MLG with improved crystallinity and uniformity at a comparatively lower temperature by SPR. Our approach is to use Co as catalyst for the fabrication of MLG and to use heat sputtering in place of conventional room temperature (RT) sputtering for the deposition of catalyst and the a-C. The extra catalyst Co will be removed from the upper surface of the fabricated MLG, so that only MLG will be obtained on n-GaN directly for further applications.

5.3. Experimental methods

5.3.1. Sample preparation

The process flow of MLG fabrication is shown in Fig. 5.1. As the substrate, commercially available n-GaN layer (purchased from POWDEC, Japan) of 1 µm thickness on 2 µm undoped GaN (u-GaN) grown on sapphire was used. The dopant for n-GaN was Si and the carrier concentration (n) was from 6 x 10^{16} to 1 x 10^{17} cm^{-3}. A buffer layer (GaN) separated u-GaN

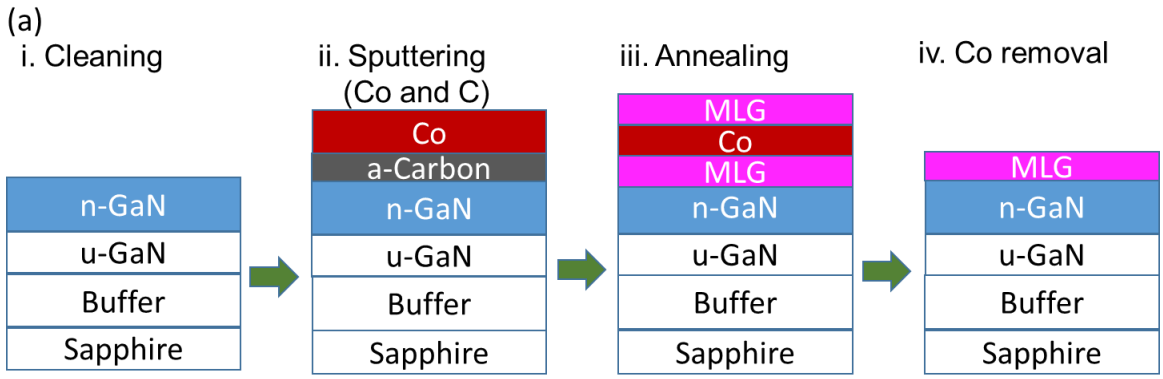


Figure 5.1. Process flow of fabrication of MLG on n-GaN by solid-phase reaction.

and sapphire. The thickness of the buffer layer was 30 nm. The n-GaN substrates were cleaned ultrasonically with tetramethylammonium hydroxide (TMAH), isopropyl alcohol (IPA), and ultrapure water. The substrates were then dipped in concentrated HCl to remove the native oxide layers and then again cleaned in ultrapure water ultrasonically and finally dried in nitrogen flow. An amorphous C layer of 40 nm thickness and a Co layer of 160 nm thickness were deposited on n-GaN by magnetron sputtering. The flow rate of Ar was 20 sccm and the pressure was 1 Pa with a base pressure of 7.0 × 10^{-4} Pa. The sputtering powers for Co and C were 100 and 400 W, respectively. The structure of the sputtered film was Co/a-C/n-GaN

(upper layer/lower layer). For the fabrication of n-GaN based SBD uniform MLG is required. We have used Co/a-C layer to fabricate MLG on n-GaN not the Co-C layer since. we have found that, by annealing of Co-C layer over SiO_2 substrate, the formation of MLG is not uniform over the entire substrate as discussed in chapter 3.

The sputtering was carried out at room temperature as well as at various temperatures between 100 and 200 ^oC at intervals of 50 ^oC. The sputtered structures were then annealed in a tube furnace at various temperatures between 600 and 750 ^oC at intervals of 50 ^oC. The annealing time was 30 min in a vacuum of 5×10^{-3} Pa. After annealing, the Co layer was removed from the upper surface using H_2SO_4 and H_2O_2 solutions.

5.3.2 Sample characterization

The structural properties of the annealed films were analyzed by Raman spectroscopy using an excitation laser of 532 nm wavelength. X-ray diffraction (XRD) analysis using Cu K_α radiation was carried out to analyze the crystal structures of annealed Co/a-C/n-GaN. The surface of the films was observed by scanning electron microscopy (SEM) and optical microscopy.

5.4. Results and discussions

5.4.1. MLG deposition on n-GaN by room-temperature (RT) sputtering and annealing

Figure 5.2 shows the Raman spectra of the RT-sputtered Co/C layers on n-GaN annealed at various temperatures ranging from 600 to 750 ^oC (a) before and (b) after Co removal. From the Raman spectra shown in Fig. 5.2, we can see that graphitization occurred at temperatures between 600 to 700 ^oC, because the spectra show distinct G, D, and 2D peaks. The G band is derived from the graphitic structure and the D band appears from disordered structures such as edges and grain boundaries [12]. MLG crystallinity is determined from the G/D ratio [13]. A higher G/D ratio indicates a higher crystallinity.

Figure 5.3 shows the comparison of G/D ratio of MLG film deposited by annealing RT sputtered Co/a-C/n-GaN layer at various temperatures between 600 and 750 ^oC. The G/D ratio was observed to increase with annealing temperature upto 700 ^oC and no distinct G and D peak were found annealing at and above 750 ^oC even after removal of Co from the upper surface of the sample. Thus, the graphitization stopped at 750 ^oC annealing of the sputtered Co/C on n-GaN. With the increase of annealing temperature, more energy was considered to be supplied for the graphitization to occur by SPR. Another noticeable point is the reduction of G/D ratio after annealing at 650 ^oC in comparison with 600 and 700 ^oC. To ensure about the reason behind

the non-graphitization at 750 °C and above and lowering of the G/D ratio at 650 °C, more characterization about the structural property is required and will be described later in this section. The maximum G/D ratio for MLG films with RT sputtering and annealing was found after annealing at 700 °C.

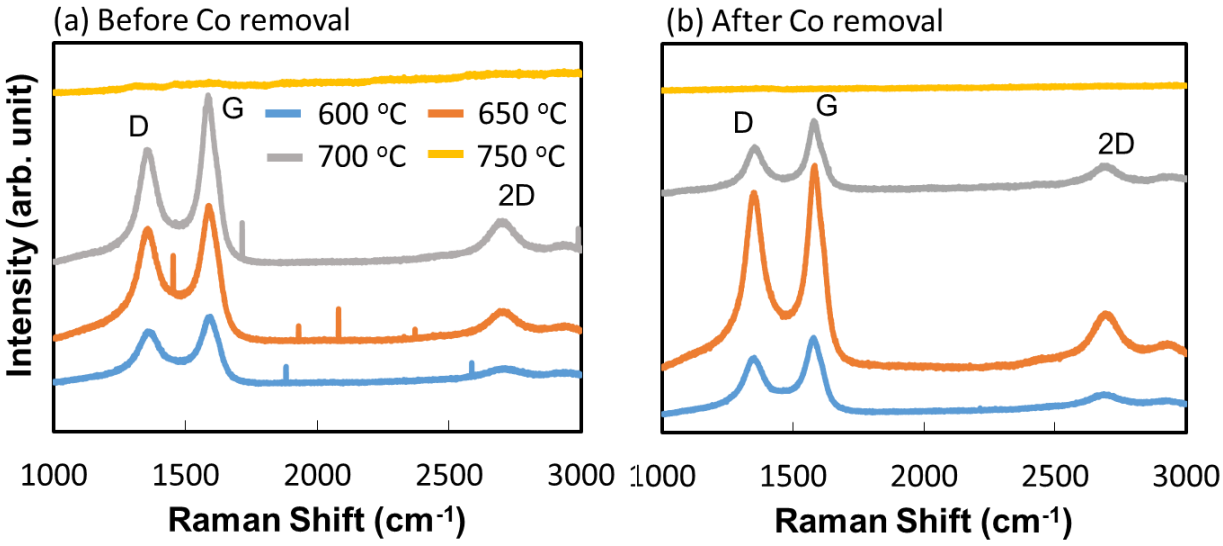


Figure 5.2. Raman spectra of MLG films deposited by annealing RT sputtered Co/Ca-C/n-GaN layer at various temperature between 600 and 750 °C (a) before and (b) after Co removal.

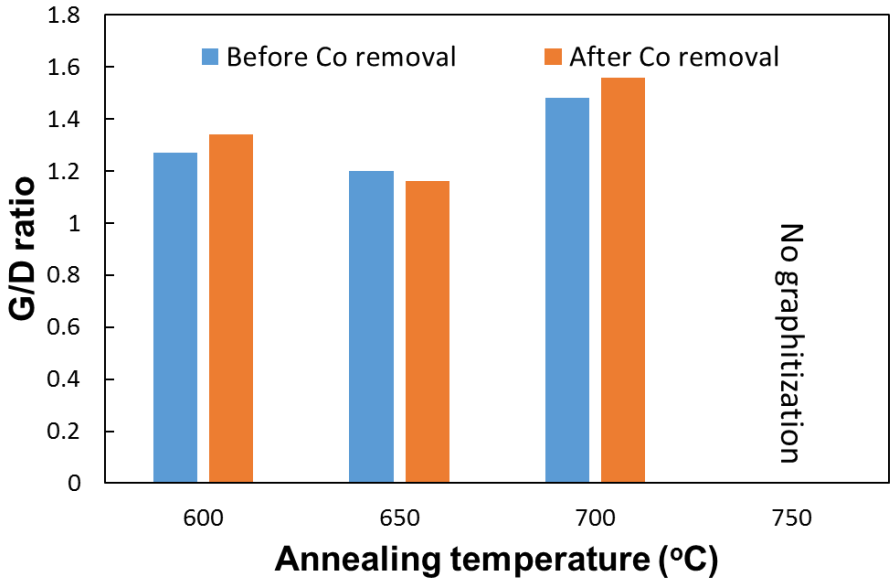


Figure 5.3. Comparison of G/D ratio of MLG films deposited by annealing RT-sputtered Co/Ca-C/n-GaN layer at various temperature between 600 and 750 °C before and after Co removal.

Fig. 5.4 shows the surface images obtained by optical microscopy for RT-sputtered Co/C layers annealed at 600 to 750 °C before Co removal. Figure 5.5 shows the surface images

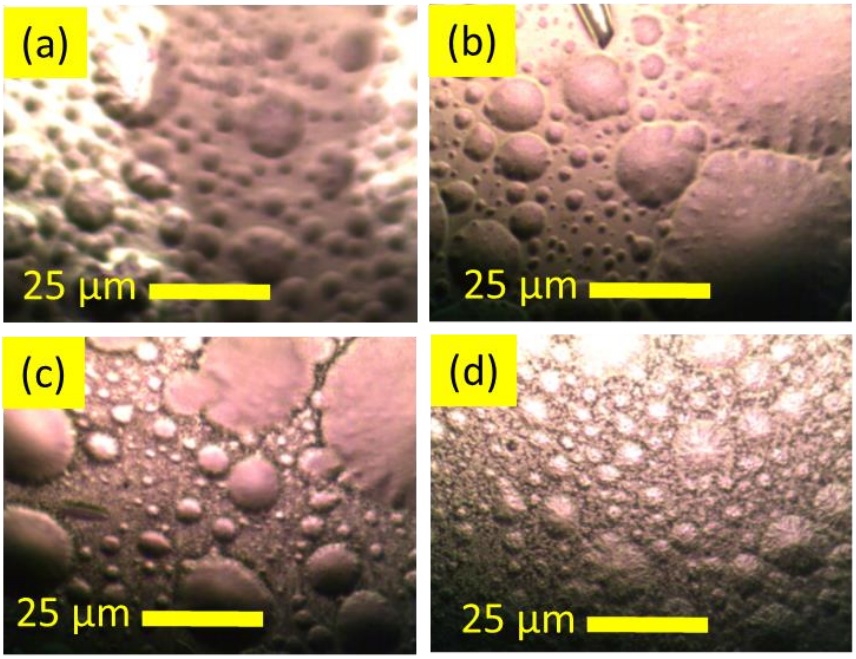


Figure 5.4. Optical microscopy image of RT-sputtered Co/C layer after annealed at (a) 600, (b) 650, (c) 700, and 750 °C before Co removal.

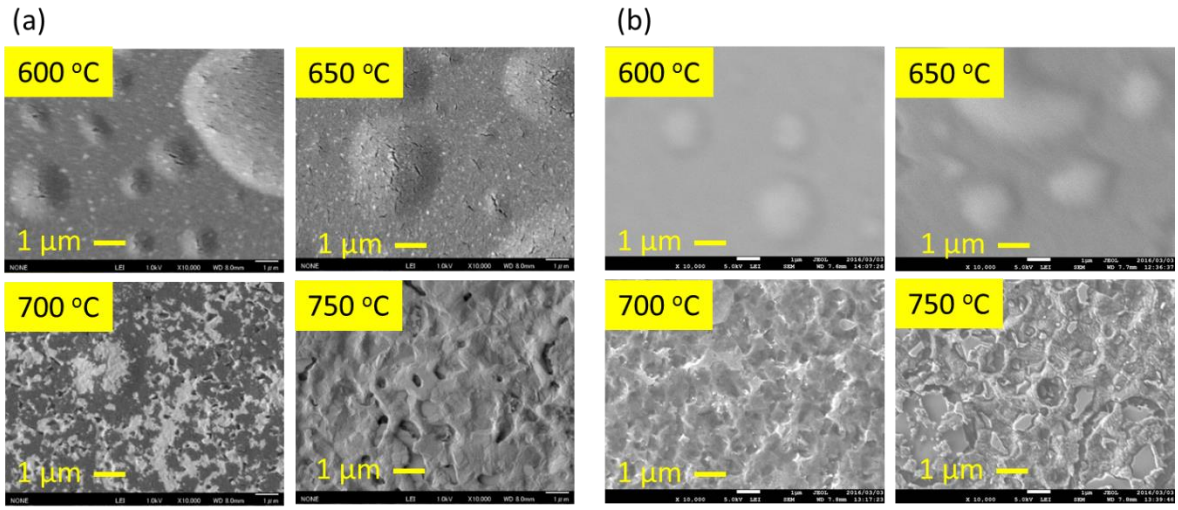


Figure 5.5. SEM images of RT-sputtered Co/C layer after annealed at various temperatures between 600 and 750 °C (a) before and (b) after Co removal.

obtained by SEM for RT-sputtered Co/C layer annealed at various temperatures between 600 and 750 °C (a) before and (b) after Co removal. From the images shown in Figs. 5.4 and 5.5, it is seen that the surfaces of the annealed films were not uniform over the entire substrate; even

after removal of Co. Rather, the sample surfaces became rough also the catalyst agglomeration occurred after annealing at and above 700 ^{o}C. The possible reasons for the non-uniformity of the sample surface might be the thermal expansion coefficient difference between GaN and Co/C and sapphire. Owing to this difference in the thermal expansion coefficient between the sputtered films, sapphire, and GaN, when the sputtered structures were annealed at a high temperature, GaN, sapphire, C, and Co would expanded to different rates, resulting in non-uniformity of the sample surface. The thermal expansion co-efficients of GaN, sapphire, Co and C is shown in Table 5.1.

Table 5.1. Thermal expansion co-efficient of GaN, C, and Co and sapphire.

Material	Thermal expansion co-efficient (mmK^{-1})
GaN	3.17×10^{-6}
C	7.0×10^{-6}
Co	12×10^{-6}
Sapphire	6.6×10^{-6}

To study the effect of annealing temperature on structural properties of the annealed Co/C/n-GaN samples, XRD measurements were carried out before removal of Co. Figure 5.6 Shows the XRD spectra (θ-2θ) of the RT sputtered Co/C layer after annealed at various temperatures between 600 and 750 ^{o}C before Co removal. From XRD spectra shown in Fig. 5.6, we can see that the Co(111) peak intensity increases with the increase in annealing temperature. The Co_3N(222) peaks appeared at 650 ^{o}C and upto 700 ^{o}C. After annealing at 750 ^{o}C the Co_3N(222) peak transforms into Co_3N(111). The $CoGa_3$(222) and CoGa(221) peaks appeared above 650 ^{o}C. The presence of CoGa and CoN peaks indicates the reaction between GaN and Co occurred. From Fig. 5, one can observe the variation of the Co_2O_3 peak intensity of the Co/a-C/n-GaN layers annealed from 600 to 750 ^{o}C. The Co_2O_3 peak intensity upon 650 ^{o}C annealing is higher than those after 600 and 700 ^{o}C annealing (barely visible in Fig. 5). The G/D ratios of the Co/a-C/n-GaN layers annealed at 600 and 700 ^{o}C were larger than that after annealing at 650 ^{o}C, as shown in Fig. 5.3. Therefore, a weak Co_2O_3 peak tends to indicate an improved MLG crystallinity, whereas a strong peak tends to indicate a degraded MLG

crystallinity. A strong Co_2O_3 peak appeared for the Co/a-C/n-GaN layer annealed at 750 ^oC, as shown in Fig. 5.6. The presence of a strong Co_2O_3 peak at 750 ^oC might be the reason for the

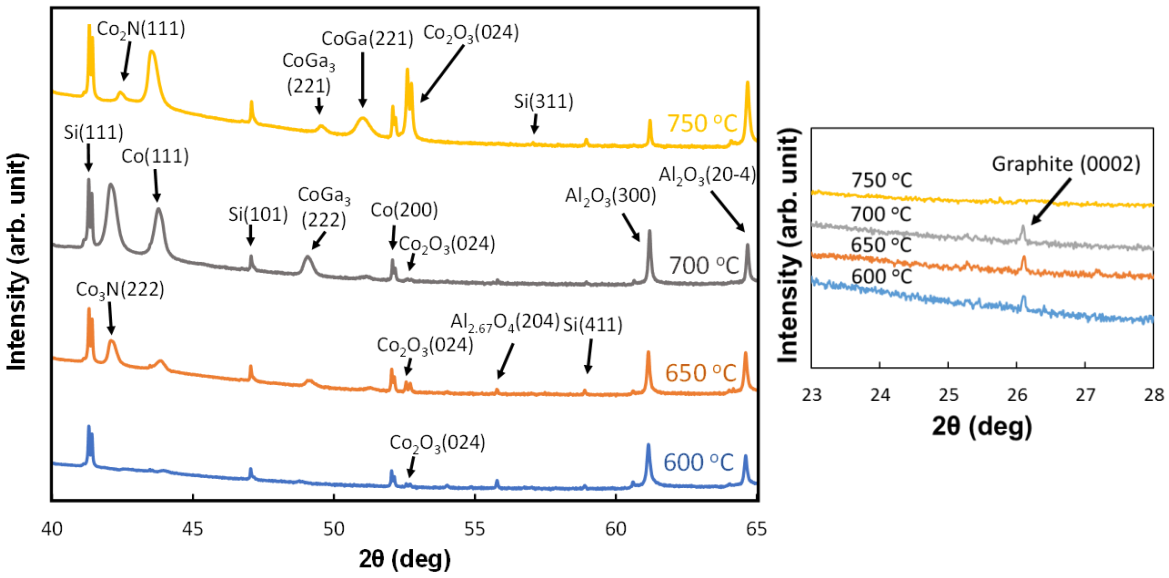


Figure 5.6. XRD spectra of RT sputtered Co/C layer on n-GaN after annealed at various temperatures between 600 and 750 ^oC before Co removal. The right hand side Fig. is for the confirmation of graphite (0002) peak.

non-graphitization, as confirmed from Raman spectra shown in Fig. 2. The intensity of the CoGa(221) peak is comparatively higher for annealing at 750 ^oC in comparison with those annealed between 600 and 700 ^oC. The enhancement of the reaction between GaN and the sputtered films might be another reason behind the non-graphitization of Co/a-C/n-GaN layer after annealed at 750 ^oC.

5.4.2 Improved MLG deposition after heat sputtering and annealing

From the optical and SEM images shown in Figs. 5.4 and 5.5, we found that MLG surface was not uniform over the entire n-GaN substrate. The surface of the annealed film was rough and there were many hillocks over the entire n-GaN substrates for RT-sputtered and annealed Co/C/n-GaN samples. For the potential application of MLG in fabricating a device, the uniformity of MLG is required. To improve the surface uniformity of MLG films the following technique of heat sputtering for the deposition of amorphous C and Co layers was applied to reduce the thermal stress between the GaN and Co/a-C layers. Heat sputtering was carried out at temperatures between 100 to 200 ^oC at an interval of 50 ^oC. In this process, the cleaned n-

GaN substrate were first allowed to heat at desired sputtering temperature with the base pressure of 7 x 10^{-4} Pa for 30 min, after that sputtering of a-C and Co was done maintaining the substrate temperature at the desired value. After finishing the sputtering, the sample was allowed to cool down to RT with the flow of Ar.

Figures 5.7 show the Raman spectra of MLG films annealed at 600 to 750 ^{o}C for (a) RT-, (b) 100-, (c) 150-, and (d) 200-^{o}C-sputtered Co/C layers after Co removal. From these Raman spectra, it is seen that the crystallinity of heat-sputtered samples annealed at and above 650 ^{o}C was improved significantly. For the RT-sputtered samples annealed at 750 ^{o}C, there was no graphitization, as can be seen from Fig. 5.7(a), in contrast, for heat-sputtered samples, graphitization occurred at 750 ^{o}C, as can be seen from the Raman spectra shown in Figs. 5.7(b) to 5.7(d). No graphitization occurred at 750 ^{o}C with RT sputtering, but graphitization occurred at 750 ^{o}C with heat sputtering; therefore, heat sputtering of Co/C improves the graphitization of Co/C on GaN in comparison with RT sputtering, even when the annealing temperature was the same.

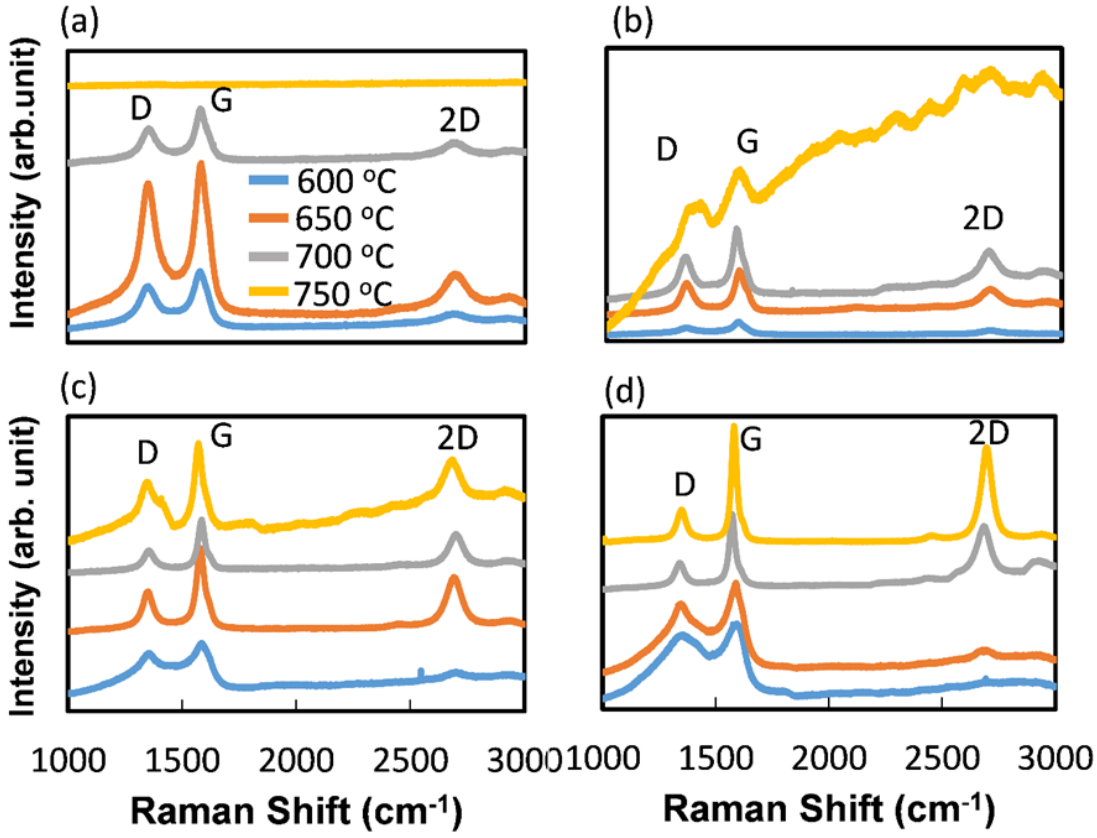
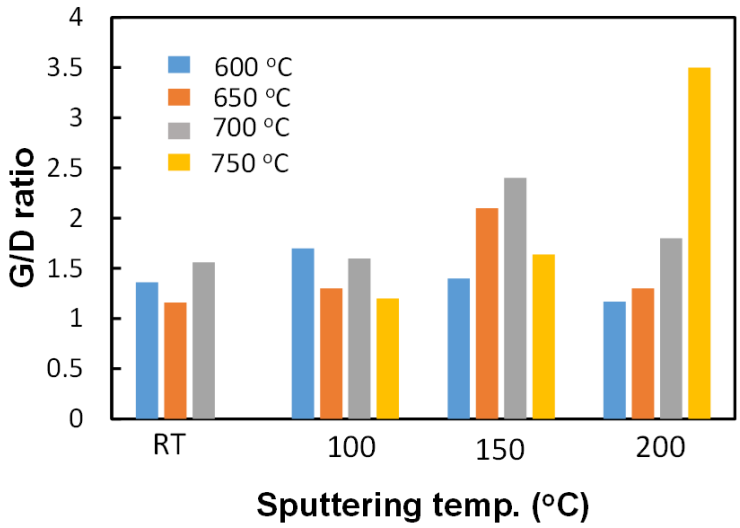


Figure 5.7. Raman spectra of MLG films deposited by annealing of (a) RT-, (b) 100-, (c) 150-, and (d) 200-^{o}C-sputtered Co/C layers at 600 to 750 ^{o}C after Co removal.



Figures 5.8. Comparison of G/D ratio of MLG films deposited by annealing of (a) RT-, (b) 100-, (c) 150-, and (d) 200-°C-sputtered Co/C layers at 600 to 750 °C after Co removal.

Figure 5.8 shows the variation of G/D ratio as a function of annealing temperature for RT-, 100-, 150-, and 200-°C-sputtered Co/C films after Co removal. From Fig. 5.8, the G/D ratios are seen to increase for heat sputtering in comparison with RT sputtering for annealing temperatures at and above 650 °C, and especially at 150 and 200 °C sputtering. The G/D ratios are seen to increase with increasing annealing temperature from 600 °C for 200 °C sputtering. The maximum G/D ratio for RT, 100, 150, and 200 °C sputtering were found to be 1.52, 1.6, 2.4 and 3.5 respectively. Several research groups as mentioned in Refs. 36-38, deposited transfer-free MLG on n-GaN substrate by CVD. The CVD temperatures were as high as 950 °C as mentioned earlier. In our present work, the deposition temperature was varied between 600 and 750 °C and for each deposition condition in case of heat sputtering MLG growth took place. Thus, we have succeeded in decreasing the deposition temperature of MLG in comparison with other available reported literatures. The MLG crystallinity i.e., the G/D ratio was less than unity with all the available reports [8-10]. In this present work the G/D ratio was greater than unity for each deposition conditions. The maximum G/D ratio was found to be 3.5 as mentioned earlier. Therefore, we also succeeded in improving the MLG crystallinity in comparison with other available reports.

Figure 5.9 shows the SEM images of the surface of the MLG films annealed at various temperatures ranging from 600 to 750 °C for (a) RT-, (b) 100-, (c) 150-, and (d) 200-°C-sputtered Co/C layers after Co removal. From the SEM images shown in Fig. 5.9, it is clear that the surface uniformity of MLG films improved with sputtering at and above 150 °C for the deposition of Co/C, in comparison with RT sputtering. There is no significant surface

improvement with 100 ^{o}C sputtering compared with RT sputtering. Sputtering at 100 ^{o}C might not be sufficient to reduce the thermal expansion difference between GaN and Co/C, as a result no significant improvement in surface uniformity was observed. The MLG film fabricated by 150 ^{o}C sputtering of the Co/C layer annealed at 650 ^{o}C showed the optimum surface condition.

The thermal expansion coefficients of GaN, C, and Co are 3.17 x 10^{-6}, 7.0 x 10^{-6}, and 12 x 10^{-6} mm/K respectively. Theoretically it was found that the difference in the thermal expansion between the GaN layer and RT-sputtered C and Co layers after annealing at 650 ^{o}C were 4.9 x 10^{-3} and 8.62 x 10^{-3} mm, respectively. On the other hand the difference in the thermal expansion between GaN layer and C and Co layers with 150 ^{o}C sputtering and annealing at 650 ^{o}C theoretically decreased to 2.9 x 10^{-3} and 3.42 x 10^{-3} mm, respectively. Thus, heat sputtering of C and Co may lead to a "decrease" in the difference in thermal expansion among GaN, C, and Co after annealing at 650 ^{o}C, which may lead to the improvement of surface uniformity. The surface roughness of the sample sputtered at 150 ^{o}C and annealed at 650 ^{o}C was also measured by laser microscopy, as shown inset of Fig. 5.9(c).

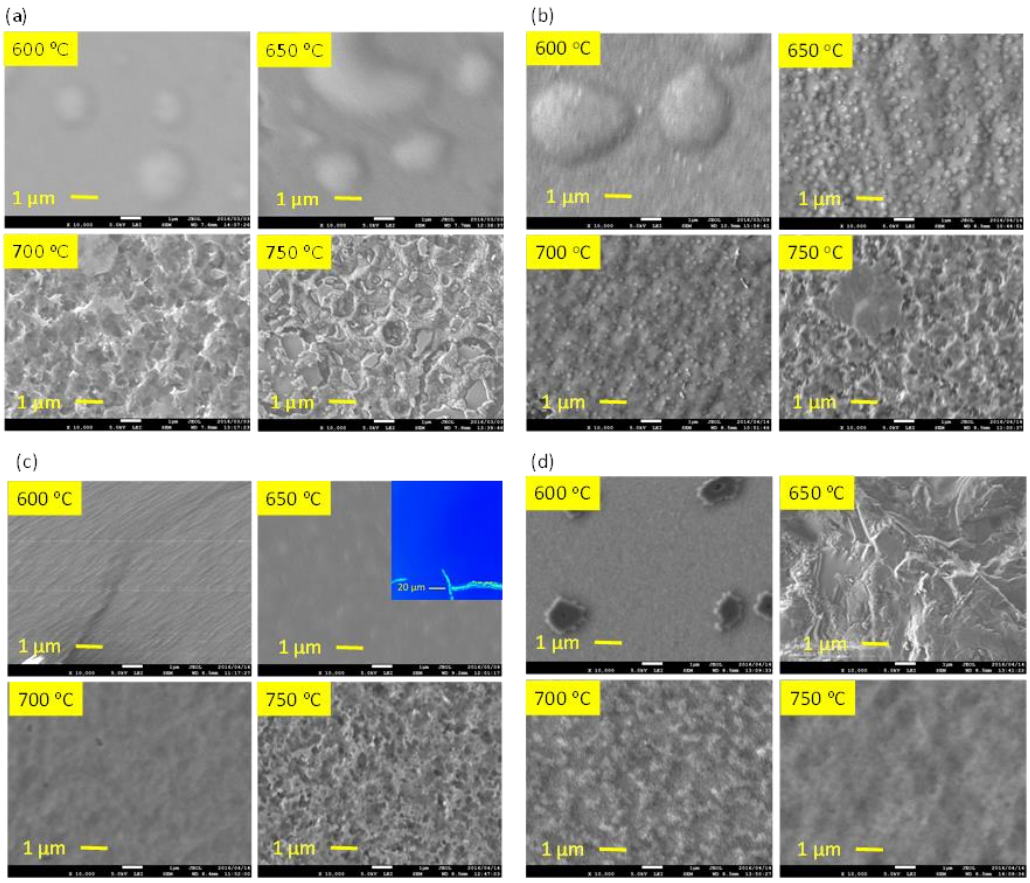


Figure 5.9. SEM images of the surface of the MLG films annealed at various temperatures ranging from 600 to 750 ^{o}C for (a) RT-, (b) 100-, (c) 150-, and (d) 200-^{o}C-sputtered Co/C

layers after Co removal. The inset of Fig. (c) is the surface uniformity as measured by laser microscopy for 150 ^{o}C sputtered Co/a-C layer annealed at 650 ^{o}C after Co removal.

Thus, heat sputtering of C and Co may lead to a "decrease" in the difference in thermal expansion among GaN, C, and Co after annealing at 650 ^{o}C, which may lead to the improvement of surface uniformity. The surface roughness of the sample sputtered at 150 ^{o}C and annealed at 650 ^{o}C was also measured by laser microscopy, as shown in Fig. 8(c). Except for some wrinkles, the surface was almost uniform, as shown as Fig. 8(c). The reduction of the difference in the thermal expansion between GaN and Co/C, and surface cleaning by heat sputtering might be the potential reasons for the improvement of surface morphology.

The growth condition for MLG films with improved crystallinity and uniformity by SPR by heat sputtering and annealing was optimized by comparing the crystallinity and uniformity as shown in Figs. 5.8 and 5.9. The optimized growth condition was 150 ^{o}C sputtering of Co/a-C layer annealed at 650 ^{o}C. From Fig. 5.8, it is seen that the G/D ratio of MLG films for 150 ^{o}C sputtering annealed at 700 (sample x) and 200 ^{o}C sputtering annealed at 750 ^{o}C (sample y) are higher than our optimized growth condition. From Fig. 5.9(c) and 5.9(d), it is seen that the surface uniformity for 150 ^{o}C sputtering and 650 ^{o}C annealing is better than sample x and y.

Figures 5.10 shows the XRD spectra of RT, 100, and 150 ^{o}C sputtered Co/a-C/n-GaN after annealing at (a) 650 and (b) 700 ^{o}C. From Fig. 5.10(a), we can see two strong peaks of Co_2N (111) and CoGa(221). The presence of these compound phase indicates that the reaction between Co and GaN has taken place upon annealing the RT-sputtered structure at 650 ^{o}C. A Co_2O_3 phase appeared for RT-sputtered Co/a-C/n-GaN layer annealing at 650 ^{o}C. It can be seen from the XRD spectra of Fig. 5.10(a) that the intensity of the Co_2O_3 peak was decreased after 100 ^{o}C-sputtered structure annealed at the same temperature and the Co_2O_3 peak almost vanished after the sputtering temperature of 150 ^{o}C. As we have discussed in the previous Sect., the MLG crystallinity was found to depend on the Co_2O_3 peak intensity. By comparing the XRD spectra of Fig. 5.10 (a) and G/D ratio comparison of Fig. 5.8 one can observe the G/D ratio fsor 100 and 150 ^{o}C sputtered layer annealed at 650 ^{o}C was higher than the RT-sputtered Co/a-C/n-GaN layer annealed at the same temperature. From Fig. 5.10 (b), one can observe the formation of Co_2N and CoGa phases for both samples with RT and heat sputtering after annealed at 700 ^{o}C. Moreover the intensity of Co_2O_3 phase become higher for 100 ^{o}C-sputtered sample in comparison with the RT-sputtered sample. However, the Co_2O_3 peak almost vanishes for 150 ^{o}C-sputtered sample annealed at the same temperature. The crystallinity of 100 ^{o}C-

sputtered sample was found to be little smaller than the RT-sputtered sample after annealing at 700 °C. On the other hand, MLG crystallinity was found to be improved for 150 °C sputtered sample than the RT-sputtered sample. Thus the reason behind the improvement of MLG crystallinity with heat sputtering in comparison with RT sputtering might be due to the reduction of Co_2O_3 phase or suppression of the reaction between GaN and Co. The effect of heat sputtering on the crystallinity and uniformity of MLG films will be discussed in details in the next section.

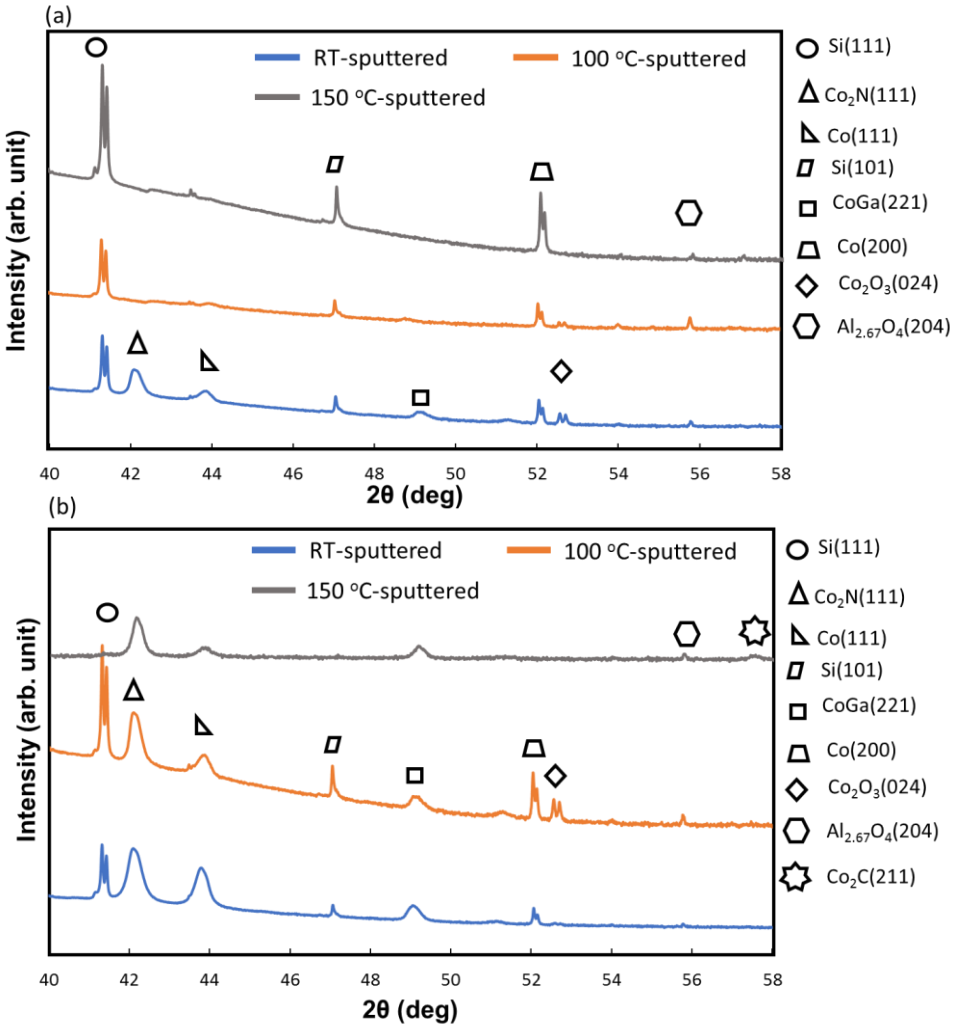


Figure 5.10. XRD spectra of RT, 100, and 150 °C sputtered Co/a-C/n-GaN after annealing at (a) 650 and (b) 700 °C.

5.4.3. Effect of Heat Sputtering

To compare the effect of heat sputtering among the samples, XRD measurements were carried out for four samples annealed at 650 °C with RT, 100, and 150 °C sputtering, and sputtered at RT with in situ annealing at 150 °C before sputtering (in situ annealed RT sputtered).

For the in situ annealed RT sputtered sample, the n-GaN substrate were annealed at 150 ^{o}C for 30 min inside the sputtering chamber and then allowed to cool down to RT and then the sputtering was done. The sputtered sample was then annealed in a tube furnace at 650 ^{o}C for 30 minutes. Figure 5.11 shows the (a) Raman spectra and (b) surface SEM image of the in

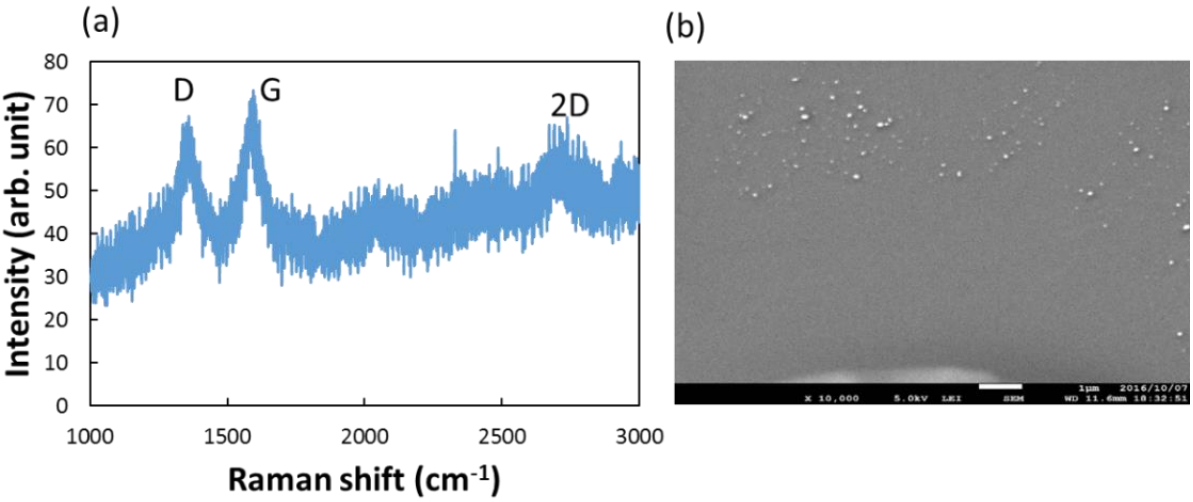


Figure 5.11. (a) Raman spectra and (b) surface SEM image of the in situ annealed RT sputtered sample annealed at 650 ^{o}C after Co removal.

situ annealed RT sputtered sample annealed at 650 ^{o}C after Co removal. From Fig. 5.11 we can see that the MLG surface uniformity was improved but the MLG crystallinity was degraded in comparison with the other samples annealed at 650 ^{o}C.

Figure 5.12 shows the XRD patterns (θ-2θ) of RT-, 150 and 150 ^{o}C in situ annealed RT-sputtered Co/C/n-GaN films annealed at 650 ^{o}C before Co removal. From the XRD spectra shown in Fig. 5.12, we can see the existence of the CoGa phases for the RT-sputtered Co/C layer annealed at 650 ^{o}C. The presence of CoGa phases in the RT sputtered samples indicates the occurrence of a reaction between GaN and Co. On the other hand, the samples with heat sputtering and in situ annealed RT sputtering at the same temperature of annealing shows reduced or vanished CoGa peaks. The reduction or the disappearance of CoGa phases indicates the suppression of the reaction between GaN and Co. Thus, heat sputtering of the Co/C layer suppressed the reaction between GaN and Co, and the formation of CoGa phases was reduced or the formed phases vanished. From the SEM image shown in Fig. 8(c), one can observe the improvement in the uniformity of the 150 ^{o}C-sputtered sample annealed at 650 ^{o}C. Also from the SEM image of the in situ annealed RT-sputtered sample annealed at 650 ^{o}C (Fig. 5.11(b), a better surface uniformity was confirmed. Therefore, suppression of the reaction between GaN

and Co might be the reason for the improved uniformity of MLG films deposited by heat sputtering or in situ annealed RT-sputtered Co/C layer annealed at 650 °C.

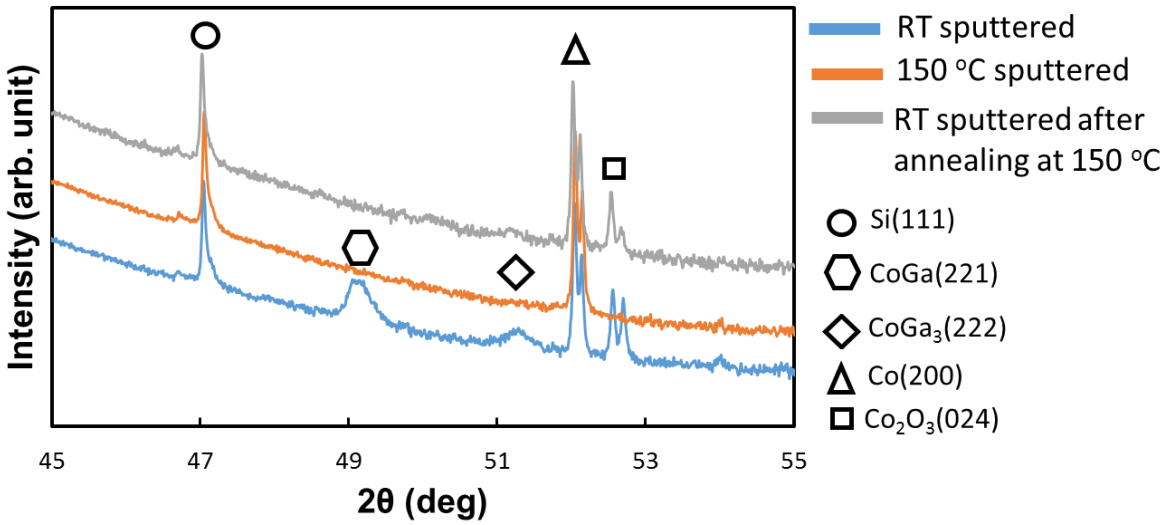


Figure 5.12. XRD patterns (θ-2θ) of RT, 100 and 150 °C-sputtered, and 150 °C in situ annealed RT-sputtered Co/C/n-GaN films annealed at 650 °C before Co removal.

Another phenomenon noted from XRD spectra shown in Fig. 5.12 is the disappearance of the Co_2O_3 phase after heat sputtering. The Co_2O_3 phase appeared even when the RT sputtering was carried on the in situ annealed sample. From the discussion in Sect. 5.3.1, it was found that the Co_2O_3 phase appearing in the RT-sputtered and 750 °C annealing samples might be responsible for the poor graphitization. From the Raman spectra of the in situ annealing RT-sputtered sample annealed at 650 °C showed the degraded MLG crystallinity as can be seen from Fig. 5.11(a). Therefore, the disappearance of the Co_2O_3 phase might be responsible for the enhanced graphitization, whereas the suppression of the reaction between GaN and Co improves the MLG crystallinity as well as uniformity. The disappearance of the Co_2O_3 phase after heat sputtering indicates the cleaning of the GaN surface before sputtering. The GaN substrates were exposed to temperatures between 100 to 200 °C in vacuum for 30 min before the sputtering was carried out. During this time, contaminants from the upper surface of GaN might be removed. The reason behind the suppression of the reaction between GaN and Co is not yet clear; further studies are required to confirm our hypothesis.

From the discussion in the above sections, the possible reasons for the improvement of MLG crystallinity and uniformity for heat-sputtered and annealed Co/C layers can be

summarized as the reduction in the difference in the thermal expansion between GaN and Co/C, the suppression of the reaction between GaN and Co, and the disappearance of the Co_2O_3 phase owing to in situ cleaning of the n-GaN surface by heat sputtering.

5.5. Summary and conclusions

For the fabrication of an MLG based n-GaN device, transfer-free deposition of MLG on n-GaN with improved crystallinity and uniformity is more promising. Also, lowering of the deposition temperature is required to minimize the C diffusion. To fabricate MLG directly on n-GaN with improved crystallinity and uniformity, we proposed MLG fabrication by SPR by annealing heat-sputtered Co/a-C layer. The effect of heat sputtering on formation, crystallinity, and uniformity of MLG in comparison with RT sputtering was discussed. The obtained results of the current chapter can be summarized as follows

- The transfer-free deposition of MLG on n-GaN by SPR with Co as a catalyst was demonstrated for the first time at a comparatively lower temperature (650 ^{o}C) than other available reports (~950 ^{o}C).
- From the characteristics obtained by Raman spectroscopy, it was found that for RT-sputtered Co/C layer annealed up to 700 ^{o}C graphitization occurred and annealing at 750 ^{o}C lead to stop the graphitization. Also, the surface of the deposited MLG was not uniform as was confirmed by SEM photograph.
- The MLG crystallinity and uniformity were improved significantly after applying heat sputtering for the deposition of amorphous C and Co layers. The growth conditions for MLG with improved crystallinity and uniformity were optimized as follows: 150 ^{o}C sputtering of the Co/C layers annealed at 650 ^{o}C.
- Decreasing the difference in the thermal expansion between GaN and Co/C, the suppression of the reaction between GaN and Co, and in situ cleaning of the GaN surface before sputtering might be the reasons for the improvement in the crystallinity and uniformity. The suppression of reaction between GaN and Co/C and the in-situ cleaning of GaN surface due to heat sputtering was confirmed by comparing thr XRD spectra among RT- and 150 ^{o}C-sputtered and 150 ^{o}C in-situ cleaned Co/C layer annealed at 650 ^{o}C.

Finally, the successful transfer-free deposition of on n-GaN with improved crystallinity and uniformity at a comparatively lower temperature was demonstrated for the first time by SPR in our present study. With further success in fabricating an MLG-GaN device, MLG deposition

on n-GaN by SPR by our proposed method might be promising for fabricating an MLG based electrode or contact without complicated transfer of MLG.

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CHAPTER SIX
FABRICATION AND CHARACTERIZATION OF A SCHOTTKY DIODE WITH TRANSFER-FREE DEPOSITION OF MULTILAYER GRAPHENE ON n-GaN BY SOLID-PHASE REACTION

6.1. Overview

In the previous chapter, we have successfully deposited transfer-free MLG films with improved crystallinity and uniformity on n-GaN substrate. To verify the applicability of the MLG films deposited by our new method, we ought to fabricate an MLG based n-GaN Schottky barrier diode (SBD). Our aim is to measure the electrical properties of the fabricated diode and compare it with other available reports. Thermal stability of the diode will also be measured and compared with conventional one.

6.2. Background and Objectives

As described in chapter 4 and 5, wide band gap semiconductor such as GaN can be used to fabricate a high performance power device such as light emitting diodes (LED) [1], metal-semiconductor-metal (MSM) photodetectors [2], high electron mobility transistors (HEMT) [3], and Schottky rectifiers [4] for high frequency and high temperature operations. For successful operation of these devices a reliable and thermally stable Schottky contact is a pre-requisite. Scientists and engineers all over the world are looking for a Schottky metal that will not be degraded during high-power and high temperature operations.

Nanocarbon (NC) materials such as graphene or multilayer graphene (MLG) can be used as an alternative Schottky metal owing to its outstanding properties and its high barrier height and low reverse leakage current has been reported by several groups [5,6]. The thermal stability of n-GaN SBD with various metal schemes such as Ni [7], TaN [8], Pt [9], Au [10], W_2B_5 [11], Cu [12] and ZrB_2 [13] has been reported. As reported for Ni [7], Cu [12], and ZrB_2 [13], the SBH of the diodes decreased after annealing at and above 500 ^oC and the diodes become ohmic the diodes become non-rectifying.

Graphene/MLG based SBD are expected to have higher thermal stability due to its high melting point and thermally stable structural properties. S. tongay et.al [14], reported the high

thermal stability of graphene or MLG/n-GaN diodes. They explained high thermal stability of graphene or MLG/n-GaN diode is due to the impenetrable barrier property against diffusion of contaminants across the interface. The detailed of diode properties including SBH and ideality factor were not reported in this literature. Therefore, still there is a lack of detailed study on the thermal stability of MLG/n-GaN Schottky diode. MLG based SBD with transfer-free deposition of MLG is more promising for improved performance [15] and to get rid of complex transfer step from another substrate. We have succeeded in fabricating transfer-free MLG on n-GaN with improved crystallinity compared to others [16,17,] as reported in the previous chapter. In this situation our objective is to fabricate a MLG/n-GaN SBD with transfer-free deposition of MLG on n-GaN by our new method. We will also measure the thermal stability of the fabricated diode and will compare with a conventional SBD.

6.3. Theoretical Study on Schottky Contact

6.3.1. Introduction

Metal – semiconductor contacts are the most important component in the structure of the semiconductor devices to be connected with the outside world. Two types of metal-semiconductor junctions are often present in each semiconductor device and involved in the fabrication of solid-state devices. The first type is the rectifying contact, which is known as Schottky contact and the second type is the non-rectifying contact that is known as Ohmic contact. The rectifying contact or the Schottky contact allows current to flow in one biasing direction and blocks current in the opposite biasing direction. This implies that the resistance of current flow in the blocking direction is very large. The Ohmic contact, on the other hand, has low resistance that allows current to flow in both biasing directions equally well. The qualities of both of types of contacts play important role in the performance of the integrated circuit devices [18]. In this section, we will discuss the properties of Shottky contact and the calculation of Schottky diode properties using I-V characteristics.

6.3.2. Schottky Contacts

Schottky contacts play an important function in all the GaN devices. An important attribute of the Schottky contact is the barrier height that is shown in the band diagram of Fig. 6.1. Part (a) of the Fig. is the metal – semiconductor junction before the contact is made between the metal and the semiconductor, and part (b) of the Fig. is the thermal equilibrium band diagram of the Schottky contact for the case of a larger work function of the metal than that of the semiconductor.

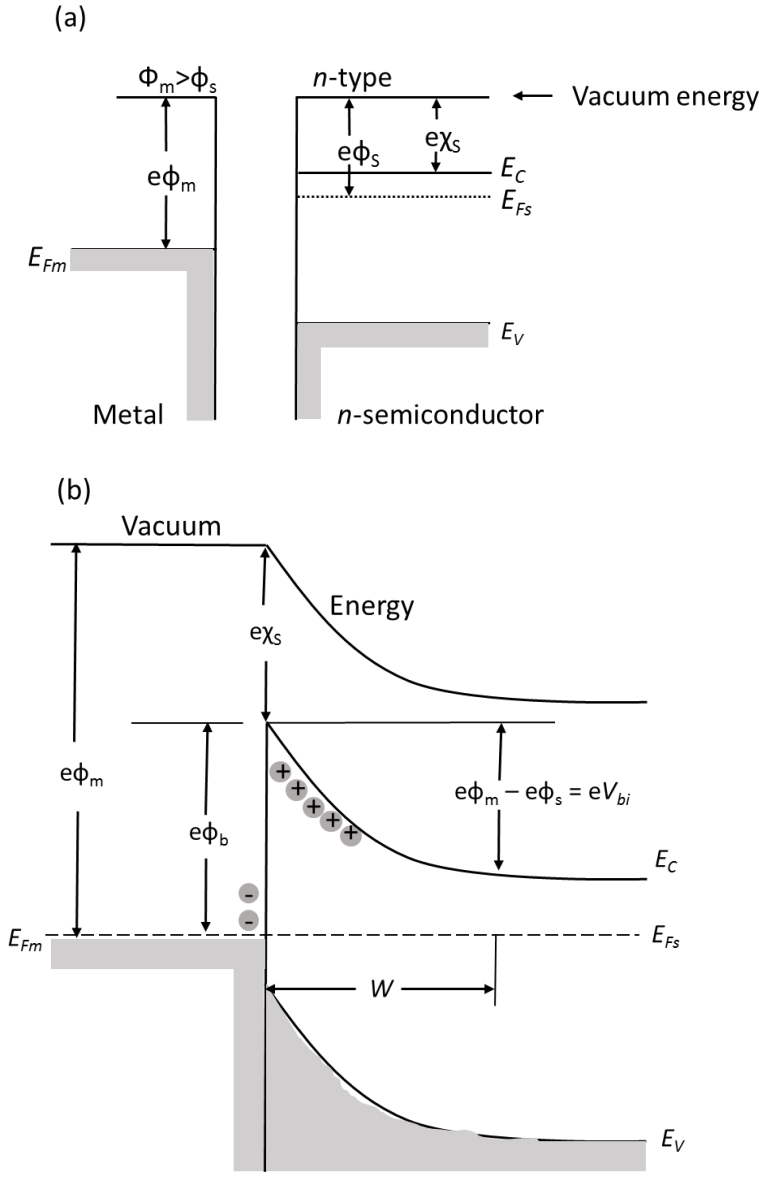

Figure 6.1. Band diagram of a metal-semiconductor junction (a) before the contact and (b) after the contact was established.

The vacuum level in the figure 6.1(a) is the reference for the band diagram. ϕ_m is the work function of the metal and ϕ_s is the work function of the semiconductor (both of the work functions are measured in volts). χ is an abbreviation for the electron affinity of the semiconductor. The fermi energy E_F represents the highest occupied electron energy state at T = 0 K in a metal; in a non-degenerate semiconductor it lies in the gap between the valance and conduction band and, as in metals, it seperates the occupied from unoccupied states at T = 0 K. E_c stands for the lowest allowed energy level for the conduction band and E_v relates to the

highest allowed energy state of the valance band. For metals the work function ϕ_m is the energy required to remove an electron at the fermi level E_{Fm} to the vacuum and has a value depending upon the type of metal. In a given semiconductor, the position of E_{Fs} depends on the type of doping: E_{Fs} is closer to E_C for n-type semiconductor and closer to E_v for p-type doping. The Metal work function and the electron affinity of some common semiconductors are shown in Table 6.1 and 6.2 [19].

Table 6.1. Work function of some commonly used metal

Metal Elements	Workfunction Values (eV)
Ag	4.26
Al	4.28
Au	5.1
Cr	4.5
Mo	4.6
Ni	5.15
Pd	5.12
Pt	5.65
Ti	4.33
W	4.55

Table 6.2. Electron affinities of some semiconductors

Semiconductor Elements	Electron affinity (eV)
Ge	4.13
Si	4.05
Cadmium telluride	4.28
GaAs	4.07
n-GaN	4.1
Aluminum gallium arsenide	3.77
Indium antimonide	4.59
Indium arsenide	4.9

When a contact between a metal with workfunction ϕ_m is established with a semiconductor having a different work function ϕ_s ($\phi_m > \phi_s$) in the example of Figs. 6.1(a) and (b), charge transfer occurs until the respective Fermi levels align at equilibrium. In the example of Fig. 6.1 (a), the different positions of the Fermi levels implies that electrons in the n-type semiconductor have an average total energy higher than that in the metal; when the contact is established the disparity in average energy causes the transfer of electrons from semiconductor

to metal. The transfer of charge results in the formation of a layer at the semiconductor interface depleted of free charge carriers, called depletion layer. The removal of electrons (similarly holes for a p-type semiconductor) leaves behind the space immobile charge of uncompensated dopant ions. The formation of a depletion region in the semiconductor is a necessary condition for the achievement of a Schottky rectifying junction. The depletion layer is shown as W in Fig. 6.1(b).

When a depletion layer is formed in the semiconductor, the space charge is mirrored a very thin layer of opposite-sign charge at the metal surface (Fig. 6.1(b)). This two layers of opposite charges, which makes the metal semiconductor junction somehow resembles to a parallel plate capacitor, give rise to an electric field and to a potential called built-in potential and is denoted as V_{bi} in Fig.6.1 (b). The corresponding energy $\phi_i = eV_{bi}$ acts as the energy barrier against the diffusion of electrons from the semiconductor to the metal.

The most important feature of the metal-semiconductor energy diagram at the equilibrium, as shown in Fig. 6.1 (b) for the n-type semiconductor, is the appearance of a discontinuity of the allowed energy states, which results in the formation of an energy barrier at the metal-semiconductor interface, ϕ_B, known as the Schottky barrier. ϕ_B is the barrier against electrons flow from the metal to the semiconductor and plays a similar role as ϕ_i with the important difference that while ϕ_i can be modified by the application of an external voltage bias, ϕ_B is unaffected by the external voltage bias. ϕ_B is called the Schottky barrier height (SBH) and can be related to the metal work function and to the semiconductor electron affinity as shown in Fig. 6.1(b)

$$\Phi_B = \Phi_m - \chi \qquad (6.1)$$

Ths equation is also known as the Schottky-Mott relation.

When a voltage is applied, the metal-semiconductor junction is no longer in equilibrium and difference in the Fermi level (E_F) position in the semiconductor and the Fermi level in the metal is determined by the applied bias. In a Schottky contact in an n-type semiconductor under a forward bias ($V > 0$) condition, which means the positive voltage applied to the metal side and the negative voltage applied to the semiconductor side, the built-in potential is reduced due to applied bias and the barrier for the electrons at the semiconductor size is reduced as a result electrons can flow easily from the semiconductor to the metal. In forward bias condition in a Schottky contact on an n-type semiconductor, the Fermi level position in the semiconductor is higher than the Fermi level position in the metal. As the forward bias is increased, the current also increases. The band diagram for a Schottky contact with forward and reverse bias is shown in Fig. 6.2 (a) and (b) respectively.

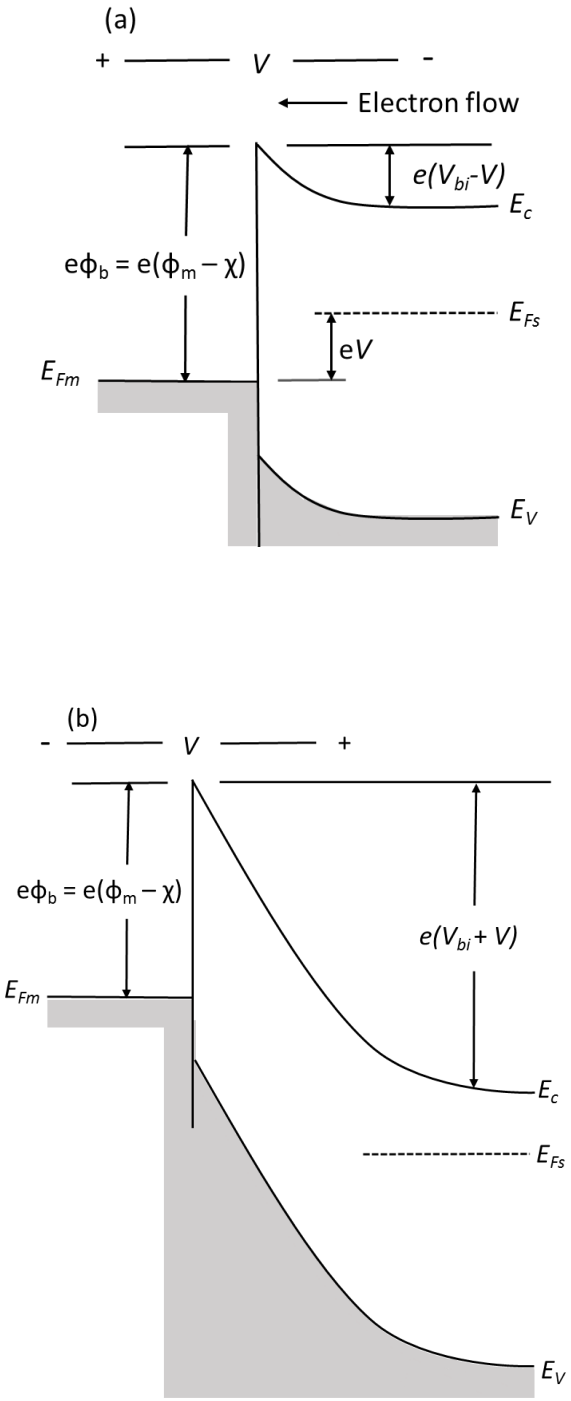

Figure 6.2. Band diagram of a Schottky contact under (a) forward and (b) reverse bias.

On the other hand, a Schottky contact on n-type semiconductor under reverse bias (V < 0), whereby positive voltage is applied to the semiconductor side and a negative voltage applied to metal side, the Fermi level position in the semiconductor is below that of the Fermi level in the metal side. Because of this, the potential increases that makes the barrier for electrons in semiconductor higher and the current from the semiconductor to the metal becomes

very small. The applied voltage does not affect the SBH and it remains constant for both bias conditions.

6.3.3. Current – Voltage relationship in Schottky contact and measurement of diode properties

Differently from a p-n junction, the current transport in a metal-semiconductor junction is mainly due to majority carriers that is to electrons from the n-type and holes for p-type semiconductors. With the moderately doped semiconductors which are employed to fabricate the Schottky diodes, the emission of thermally excited electrons or holes from the semiconductor to the metal (thermionic emission (TE)) over potential barrier is the dominating process contributing to the metal-semiconductor junction current. Other conduction mechanisms are thermionic filed emission (TFE) and field emission (FE), which include tunneling through the barrier. The relative contribution of the conduction mechanism depends on the doping concentration N in the semiconductor as well as on the temperature by defining a tunneling parameter [20,21]

$$E_{00} = \frac{eh}{4\pi}\sqrt{\frac{N}{\varepsilon_s m^*}} \qquad (6.2)$$

m* is the carrier effective mass following ref. [26,27], the conditions

$$\frac{E_{00}}{kT} \leq 0.2$$

$$0.2 < \frac{E_{00}}{kT} \leq 5, \qquad (6.3)$$

$$\frac{E_{00}}{kT} > 5$$

Categorize the dominating mechanism as TE, TFE or FE respectively. According to Eq. 6.2, at room temperature, n-type GaN substrate with N ~ 1 * 10^{17} cm^{-3} fit the first category. Thus, we will consider TE model for the calculation of diode characteristics.

The general diode equation by TE given by [22],

$$I = I_0\left[\exp\left(\frac{qV}{nkT}\right) - 1\right], \qquad (6.4)$$

where I_0 is the saturation current. Here I_0 is given by

$$I_0 = AA^*T^2 \exp\left(-\frac{q\phi_B}{kT}\right), \qquad (6.5)$$

where A is the Schottky contact area, A^* is the Richardson constant (26.4 A/(cm.K)^2 [23], q is the charge of electron, n is the ideality factor, ϕ_B is the SBH, k is the Boltzman constant and T is the temperature.

Taking logarithm on Eq. 6.4

$$lnI = \frac{qV}{nkT} + lnI_0 \qquad (6.6)$$

From the slope and intercept of *V* vs *lnI* plot, I_0 and n can be calculated. Using the value of I_0 and Eq. 6.5, ϕ_B can be calculated as follows

$$\phi_B = \frac{kT}{q}\ln\left(\frac{AA^*T^2}{I_0}\right) \qquad (6.7)$$

$$n = \frac{1}{slope\ kT/q} \qquad (6.8)$$

To have Schottky diode operating optimally, the following conditions are to be satisfied

- The ideality factor should equal to one.
- Large breakdown voltages.
- High switching speed.
- Small turn-on voltage.
- Very short time for reverse recovery (pico- or nano-second).

6.3.4. Calculation of diode properties using Cheung's and Norde function.

Cheungs function can be applied to calculate the diode properties including SBH, ideality factor, and series resistance. This method is effective in calculating the diode properties in the cases that we cannot ignore the series resistance. The Cheung's function can be written as [24],

$$\frac{dV}{d(lnI)} = \frac{nkT}{q} + IR_S \qquad (6.9)$$

$$H(I) = V - \left(\frac{kT}{q}\right)\ln\left(\frac{I}{AA^*T^2}\right) \qquad (6.10)$$

And H(I) is given as follows

$$H(I) = n\phi_B + IR_S \qquad (6.11)$$

H(I) is the sum of potential by Schottky barrier (ϕ_B) and potential drop by series resistance. From the slope and intercept of dV/d(lnI) versus I plot one can calculate R_s and n, whereas from the slope and intercept of H(I) versus I one can calculate R_s and ϕ_B.

Norde proposed an emperical function to calculate the SBH and the series resistance for a Schottky barrier diode [25] and it is another method to calculate the series resistance. We used both Cheung's function and Norde plot evaluating the series resistance. The Norde function is defined as:

$$F(V) = \frac{V}{\gamma} - \frac{kT}{q}\ln\left(\frac{I(V)}{AA^*T^2}\right) \qquad (6.12)$$

Where, F(V) is the potential drop across the junction and $\frac{V}{\gamma}$ is the applied voltage and 2nd term corresponds to the potential drop against series resistance. γ is an integer whose value is greater than the ideality factor and I(V) is the current obtained from forward bias I-V plot. The

basic technique of Norde method is to plot the proposed function with respect to the voltage applied across the SBD, and to obtain its minimum. Once the minimum of the F(V) versus V plot is determined, the value of SBH and series resistance can be calculated using the following equations

$$\phi_B = F(V_{\min}) + V_{\min} - \frac{kT}{q} \quad (6.13)$$

$$R_S = \frac{kT(\gamma - n)}{qI} \quad (6.14)$$

Where, $F(V_{min})$ is the minimum value of F(V) and V_{min} is the corresponding voltage and I is the corresponding current.

The diode properties including SBH, ideality factor, series resistance etc were calculated by using the above mentioned techniques. The comparison of the diode properties using the various methods gives the accuracy of calculation.

6.4. Experimental Methods

The process flow of fabrication of MLG on n-GaN and MLG/n-GaN (upper/lower) Schottky diodes are shown in Figs. 6.3(a) and 6.3(b), respectively. As the substrate, commercially available Si doped n-GaN layer of thickness 1μm on 2 μm undoped-GaN (u-GaN) grown on sapphire (purchased from POWDEC, Japan) were used. According to the makers information, a buffer layer of thickness 30 nm separates the u-GaN and sapphire. The carrier concentration was 6.0×10^{16} to 1.0×10^{17} cm^{-3}. The n-GaN substrates were cleaned ultrasonically with tetramethyl ammonium hydroxide (TMAH), iso-propyl alcohol (IPA) and ultrapure water. The substrates were then dipped in concentrated HCl to remove the native oxide layers and then again cleaned in ultrapure water ultrasonically and finally dried with flow of nitrogen. Amorphous C (a-C) layer of 40 nm and Co layer of 160 nm thickness were deposited on n-GaN by magnetron sputtering. The flow rate of Ar was 20 sccm and the pressure was 1 Pa with a base pressure of 7.0×10^{-4} Pa. The sputtering powers for Co and C were 100 and 400 W, respectively. The structure of the sputtered film was Co/C/n-GaN. The sputtering was carried out at temperature of 150 ^{o}C. The sputtered structures were then annealed in a tube furnace at 650 ^{o}C. The growth conditions for crystalline and uniform MLGs were optimized as 150 ^{o}C sputtered a-C and Co annealed at 650 ^{o}C and has been described in chapter 5. The annealing time was 30 minutes in vacuum of 5.0×10^{-3} Pa. After annealing, Co layer was removed from the upper surface by H_2SO_4 and H_2O_2 solution. The MLG/n-GaN diodes were fabricated with the optimized growth of MLG on n-GaN as discussed above.

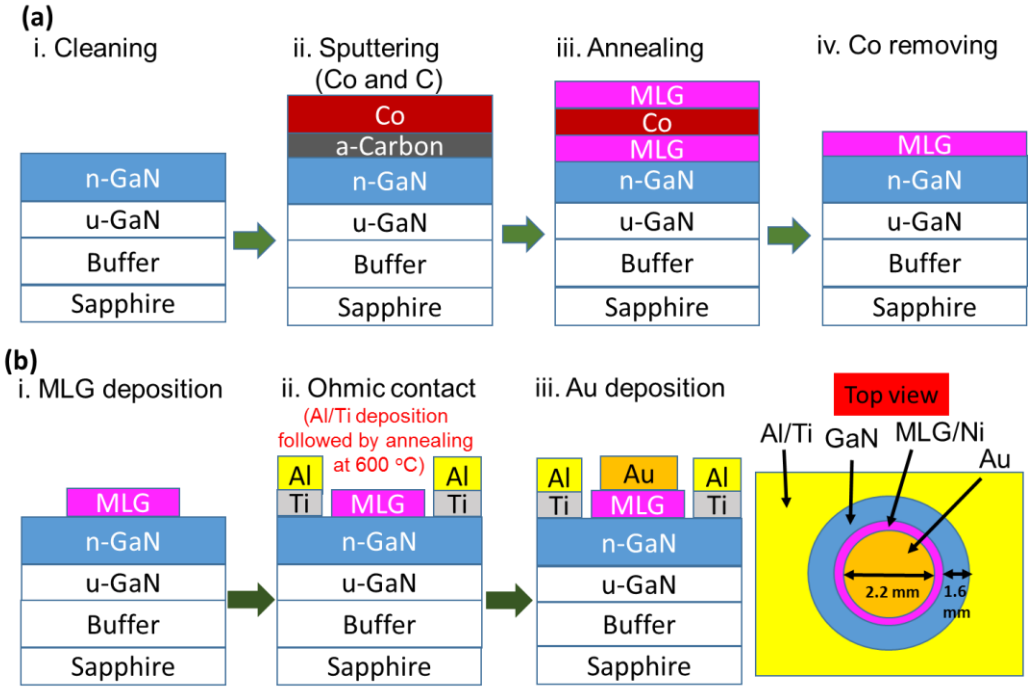

Figure 6.3. Process flow of fabrication of (a) transfer-free MLG on n- GaN by solid-phase reaction and (b) MLG/n-GaN Schottky diode and top view of the diode.

For the fabrication of MLG/n-GaN diode, circular pattern of MLG of diameter 2.8 mm was deposited and isolated at the center of the n-GaN substrate. The thickness of the MLG layer was 38±2 nm as measured by laser microscopy (not shown). Al/Ti layers of 115/35 nm thickness were deposited on n-GaN substrate by vacuum evaporation. The deposited structure was then annealed at 600 ^{o}C for 5 minutes for the formation of ohmic contact. Finally, Au layer of 150 nm thickness and 2.2 mm diameter was deposited on the MLG layer. Au/Ni layers of 150/40 nm thickness were deposited for the fabrication of the reference diode. For reference Au/Ni diodes, the annealing for the ohmic contact were performed after depositing Al/Ti prior to the Au/Ni deposition. The top view of the fabricated device is shown in Fig. 6.3 (b). The spacing between Schottky and ohmic contact was 1.6 mm. To confirm the thermal stability, the fabricated diodes were annealed at 200 to 500 ^{o}C at an interval of 100 ^{o}C in vacuum of 5 x 10^{-3} Pa for 10 minutes. The I-V characteristics of the dides without annealing and after each annealing were measured.

The structural properties of the MLG films were analyzed by Raman spectroscopy using an exciting laser of 532 nm wavelength and X-ray diffraction (XRD) analysis using CuK_{α} radiation. The surfaces of the films were observed by laser microscopy and scanning electron

microscopy (SEM). The electrical properties were measured using a semiconductor parameter analyzer (HP4155A).

6.5. Results and Discussion

6.5.1. Structural and surface characteristics of MLG

Figure 6.4 shows the (a) Raman spectra, (b) Optical, and (c) SEM images of the MLG film deposited with 150 ºC sputtered Co/C layer annealed at 650 ºC. The MLG crystallinity was confirmed from the Raman spectra shown in Fig. 6.4(a) as the spectra was characterized by distinct G, D, and 2D peaks and the G/D ratio was 1.5. From the OM and SEM images it is seen that the surface of the film is almost uniform except the SEM image consists of some white spots. To be confirmed about the composition electron probe micro analyzer (EPMA)

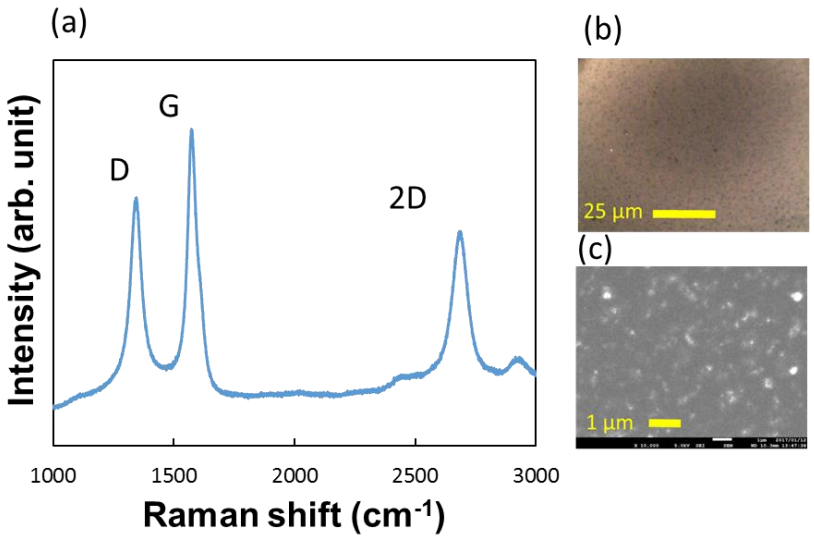

Figure 6.4. (a) Raman spectra, (b) optical, and (c) SEM image of MLG film deposited with 150 ºC sputtered Co/C layer annealed at 650 ºC.

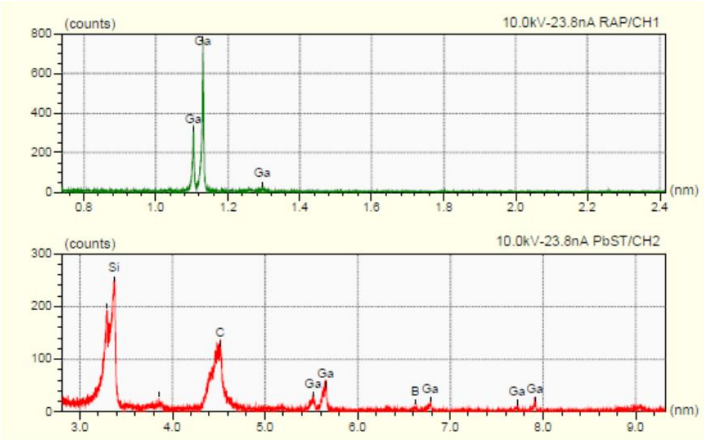

Figure 6.5. EPMA analysis of MLG film deposited with 150 ºC sputtered Co/C layer annealed at 650 ºC.

Measurements was also carried out. Figure 6.5. EPMA analysis of MLG film deposited with 150 ºC sputtered Co/C layer annealed at 650 ºC. From the EPMA analysis, the presence of Ga, Si, and C was detected. Therefore, the fabricated MLG is free from any unwanted contaminants.

6.5.2. Electrical Characteristics of as Deposited MLG/n-GaN Diode

The formation of ohmic contact was confirmed first by measuring the current-voltage (I-V) characteristics of the Al/Ti contact which is divided by gap as shown inset of Fig. 6.6. Figure 6.6 shows the I-V characteristics of the Al/Ti ohmic contact for as deposited and 600 ºC annealed structure. The resistivity of the ohmic contact was seen to be decreased significantly after annealing at 600 ºC for 5 mins in vacuum of 5×10^{-3} Pa. The forward and reverse bias I-V characteristics was found to be linear after annealing. The ohmic contact should not be affected by annealing for the thermal stability test of the diodes up to 500 ºC.

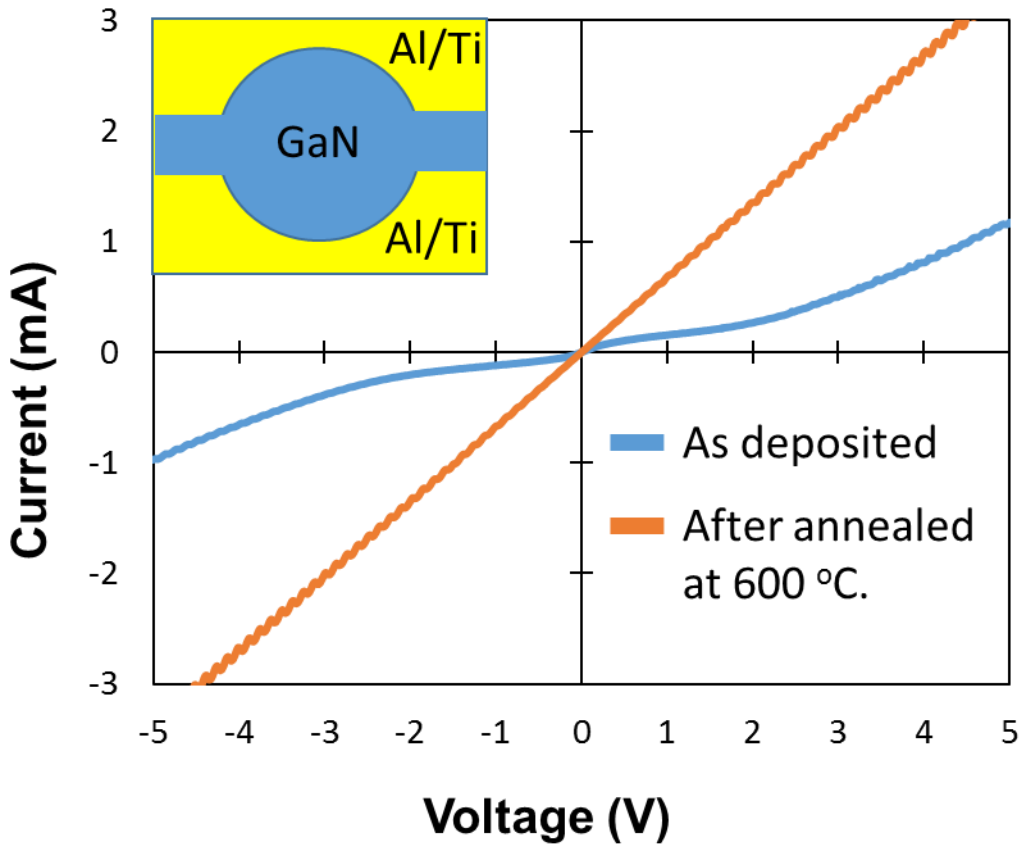

Figure 6.6. I-V characteristics of the Al/Ti ohmic contact without annealing and after annealed at 600 ºC for 5 mins.

The electrical characteristics of the as deposited diodes were measured by measuring the I-V characteristics of the diode just after fabricating the diodes. Thermionic emission (TE) model was applied to calculate the diode properties such as the SBH and the ideality factor.

Figure 6.7 shows the I-V characteristics of the fabricated Au/MLG/n-GaN diode within the voltage limit -2 to +2 Volts. The diode properties were extracted by plotting and linear fitting

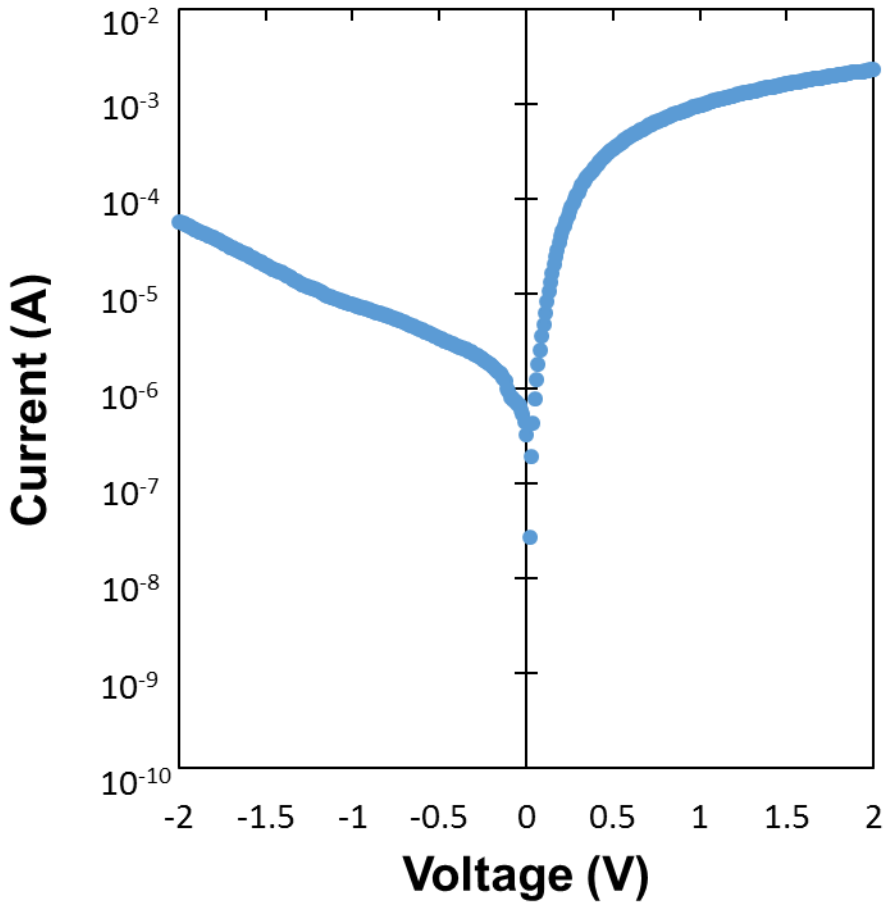

Figure 6.7. Plot of I-V characteristics of the fabricated Au/MLG/n-GaN diode within the voltage limit -2 to +2 V.

of V vs lnI curve within the voltage limit 0 to 0.3 V in the forward bias region. Figure 6.8 shows the plot of lnI as a function of forward bias voltage. The value of the saturation current I_0 can be calculated from the intercept of the plot ($\ln I_0$ = intercept). The value of SBH can be calculated by calculating the value of I_0 and using Eqn. 6.7. The ideality factor value can be calculated from the slope of the V vs lnI plot and using Eqn.6.8. The SBH and the ideality factor was found to be 0.72 eV and 1.52. The value of SBH found in our study was found to be in good agreement with available reported values [6,14]. S. Tongay et.al [6], studied the rectification of graphene-semiconductor interface and reported a SBH of 0.73 eV for graphene/n-GaN diode. On the other hand S. Tongay et. al [14], studied on the stability of graphene/GaN diodes at elevated temperatures and reported the SBH and ideality factor value

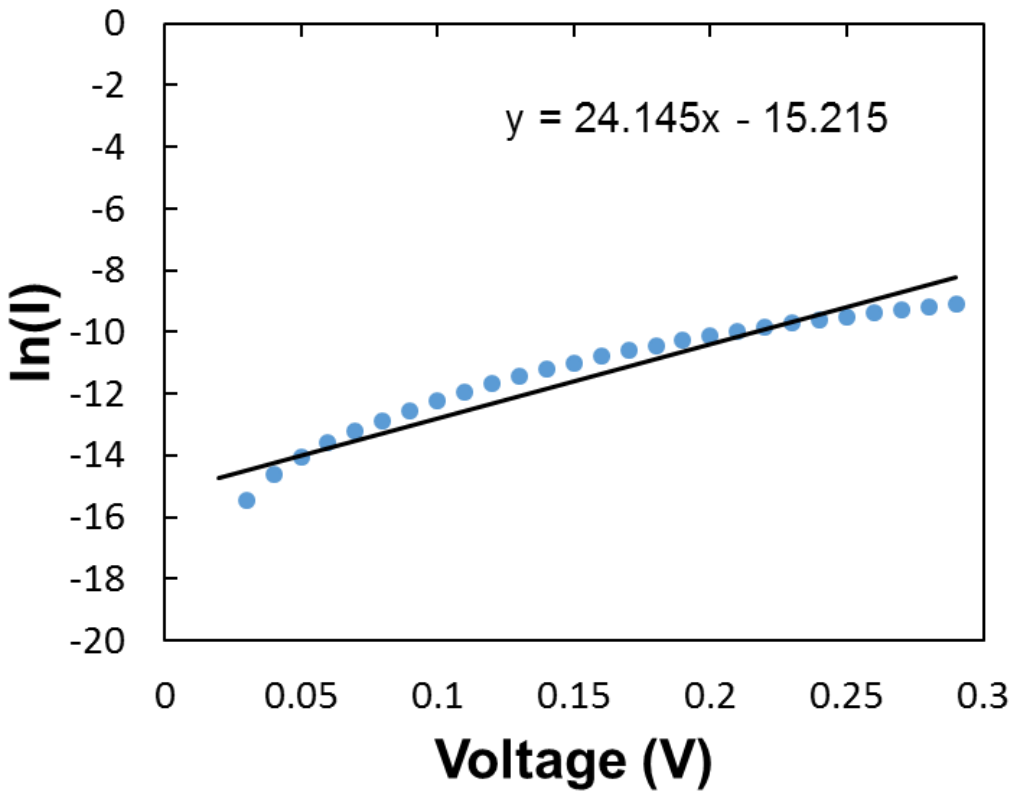

Figure 6.8. Plot of lnI as a function of forward bias voltage of Au/MLG/n-GaN diode within the voltage limit 0 to 0.3 V.

for as deposited diode as 0.74 and 2.9 respectively. Important point to be noted that the ideality factor values was as high as 2.9. In Refs. 6 and 14, the proper explanation on the values of SBH and ideality factor is somehow limited. On the other hand, S. Kim et. al [5], reported the SBH and ideality factor for graphene/GaN Schottky diode to be 0.90 and 1.32 as determined by TE model. Thus, graphene/GaN diodes shows rectification as was reported but, there is a large variation of SBH among the reported literatures. The Schottky diode properties are largely dependent on the surface treatment of the n-GaN substrate. The variation in the SBH among the reported literatures might be due to the variation in the surface treatment conditions. However, as far as the rectification at n-GaN interface is only reported for graphene. In our present study we have fabricated the diode with MLG as the Schottky contact. Our obtained results has a good agreement with the reported results, therefore, not only graphene but also MLG shows rectification at the n-GaN interface. The theoretical SBH can be calculated by using Schottky-Mott relation as shown in Eqn. 6.1. The theoretical work function of graphene is approximately 4.5 eV and the electron affinity of n-GaN is 4.10 eV. In this context the SBH

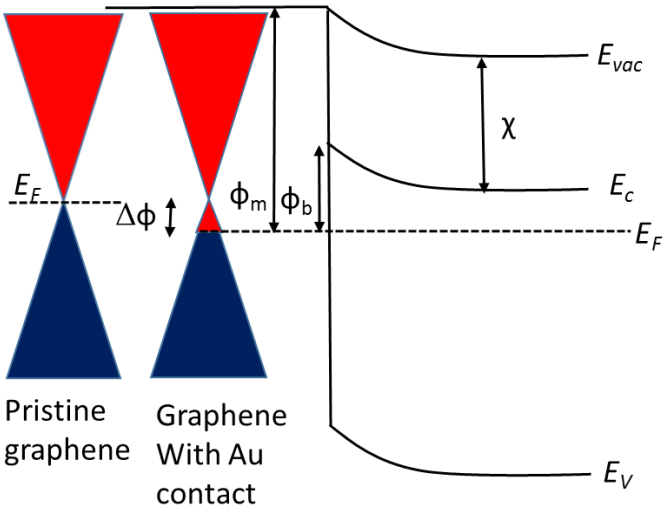

Figure 6.9. Band diagram of pristine graphene and graphene with Au contact.

value for the fabricated MLG/n-GaN diode should be equal to 0.40 eV followed by Eqn. 1. So our obtained value is deviated largely from the Schottky-Mott relation. Kumar et. al. [26], reported on the electrical properties of graphene/GaN SBD and found the SBH to be 0.60 eV which is also deviated from the theoretical SBH calculated by Schottky-Mott relation. They have explained the larger SBH of fabricated Au/MLG/n-GaN diode as the shift of graphene fermi level due to interaction with Au. When Au layer is deposited on the MLG layer as top contact the interaction between Au and graphene is considered as the effect of hole doping [27,28]. As a result of hole doping the fermi level of graphene shifted downward as shown in Fig. 6.9. The SBH is thus considered as the sum of theoretical SBH and the fermi level shift. The calculated fermi level shift of graphene due to graphene-Au interaction was found to be 0.31 eV. In this context the real SBH should be equal to the sum of theoretical value and 0.31 eV which is equal to 0.71 eV. This value surprisingly agreed very much to our calculated value 0.72 eV. Therefore, the calculated SBH of our fabricated diode agreed with some available reported theoretical values.

One of the important advantage of our method is the transfer-free deposition of MLG for the fabrication of the device in comparison with those requires transfer of graphene for the device fabrication as reported by other groups in Refs. 5,6 and 14..

6.5.3. Thermal Stability Comparison between Au/MLG/n-GaN and Au/Ni/n-GaN diode

6.5.3.1. Thermal stability comparison by thermionic emission (TE) model.

To measure the thermal stability of the fabricated diodes, the I-V measurements were made after annealing the diodes at temperatures between 200 to 500 ^{o}C in vacuum as described earlier in the experimental section. Figure 6.10 shows the I-V characteristics of (a) MLG/n-GaN and (b) Ni/n-GaN diodes without annealing and after annealed at various temperatures ranging from 200 to 500 ^{o}C. From the I-V characteristics of Fig. 6.10, we can see that the forward bias characteristics of MLG/n-GaN diode was almost similar for annealing from 200 to 500 ^{o}C. On the other hand, the I-V characteristics of the Ni/n-GaN diode was changing with annealing temperature. For annealing at 500 ^{o}C the Ni/n-GaN diode became non-rectifying, whereas the MLG/n-GaN diode shows rectification even after annealing at 500 ^{o}C. Therefore, the MLG/n-GaN diode shows better rectification property than Ni/n-GaN diode after annealing at 500 ^{o}C. We have confirmed the reproducibility of the electrical property of the diodes by measuring the I-V characteristics of 4 diodes with identical experimental conditions.

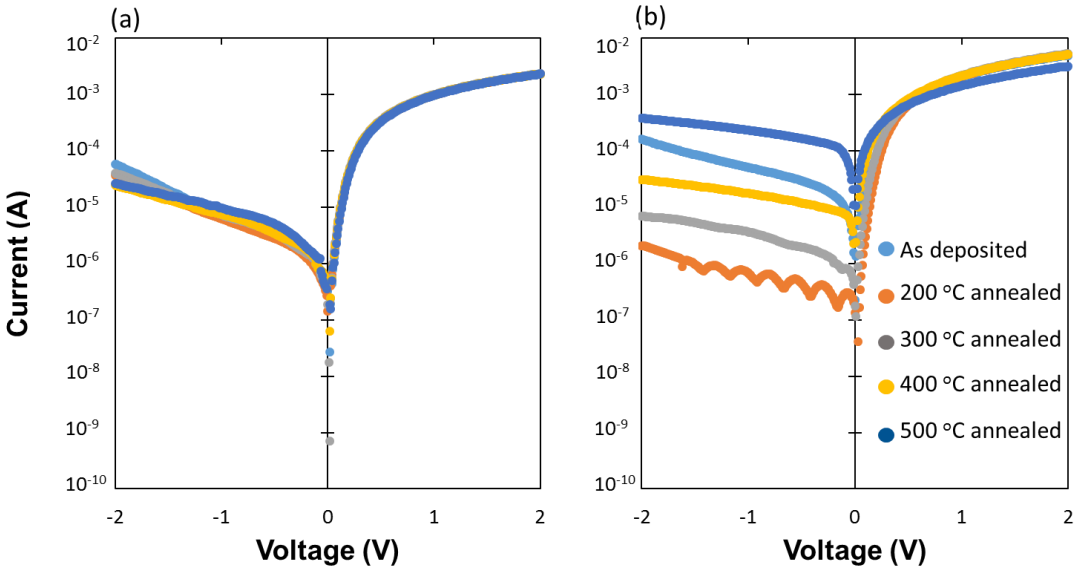

Figure. 6.10. I-V characteristics of (a) MLG/n-GaN and (b) Ni/n-GaN diode without annealing and after annealed at various temperatures ranging from 200 to 500 ^{o}C.

The electrical properties such as the SBH and the ideality factor was calculated by TE model and is described in Sect. 6.3.3. Figure 6.11 shows the variation of (a) Schottky barrier height (SBH) and (b) ideality factor (n) derived by TE model of MLG/n-GaN and Ni/n-GaN Schottky barrier diodes without annealing and after annealed at various temperatures ranging from 200 to 500 ^{o}C. From Fig. 6.11(a), we can see that the MLG/n-GaN diodes showed small variation of SBH values for annealing up to 500 ^{o}C. On the other hand, the SBH of Ni/n-GaN

diode was found to be increased for annealing at 200 °C and decreased with annealing at and above 300 °C. Moreover, the Ni/n-GaN diode showed poor rectification after annealed at 500 °C and the diode became nearly ohmic as was also observed by other research group [29], The SBH of MLG/n-GaN diode was higher and more stable than the Ni/n-GaN diode after annealing at and above 300 °C. From Fig. 6.11(b), the ideality factor values for the MLG/n-GaN diode was found to be smaller than Ni/n-GaN diode that indicates MLG/n-GaN Schottky contact was soundly formed. The value of SBH and ideality factor was seen to vary inversely i.e., higher the SBH lower the ideality factor and vice-versa. However, the ideality factor values were larger than unity for both the diodes. The high value of ideality factor might be due to the fact that the conduction mechanism is not perfectly thermionic emission or due to high series resistance (R_s) [30].

6.5.3.2. Thermal stability comparison by Cheungs function (CF).

Because for diodes with higher R_s, Cheung's function is more accurate to determine the diode

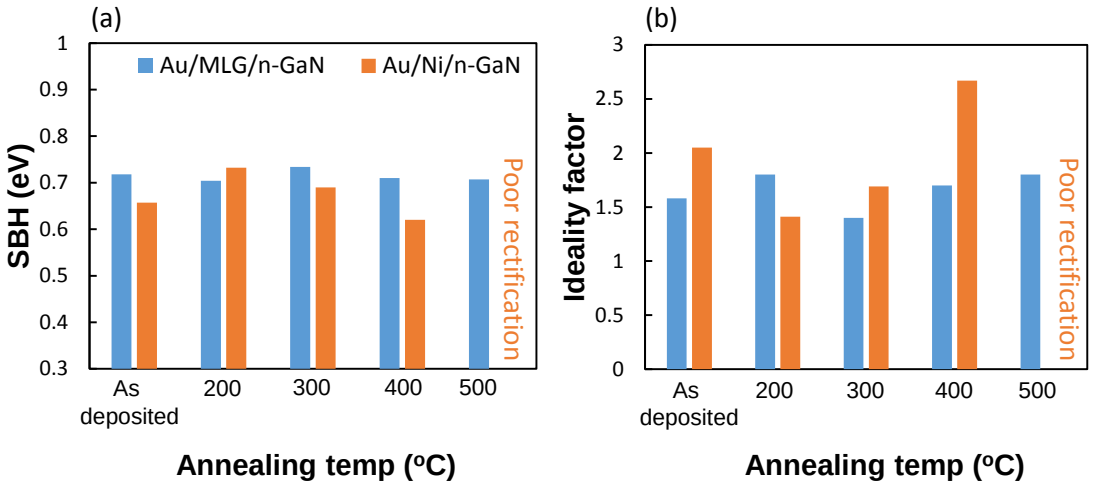

Figure 6.11. Comparison of (a) SBH and (b) Ideality factor of MLG/n-GaN and Ni/n-GaN diodes as measured by TE model without annealing and after annealed at various temperatures ranging from 200 to 500 °C.

characteristics [31], we have analyzed our results also by Cheung's function. The detailed ofdiode property calculation by Cheung's function is explained in Sect. 6.3.4. Figure 6.12 shows the plot of dV/d(lnI) vs I for (a) MLG/n-GaN and (b) Ni/n-GaN diodes without annealing and after annealed at various temperatures ranging from 200 to 500 °C. From Fig. 6.12(a), it is seen that the variation of dV/d(lnI) vs I for MLG/n-GaN diode is not much affected by annealing temperature. The value of R_s and the ideality factor was extracted from this plot after

linear fitting of the curves. Figure 6.13 shows the plot of H(I) vs I for (a) MLG/n-GaN and (b) Ni/n-GaN diodes without annealing and after annealed various temperatures ranging from 200

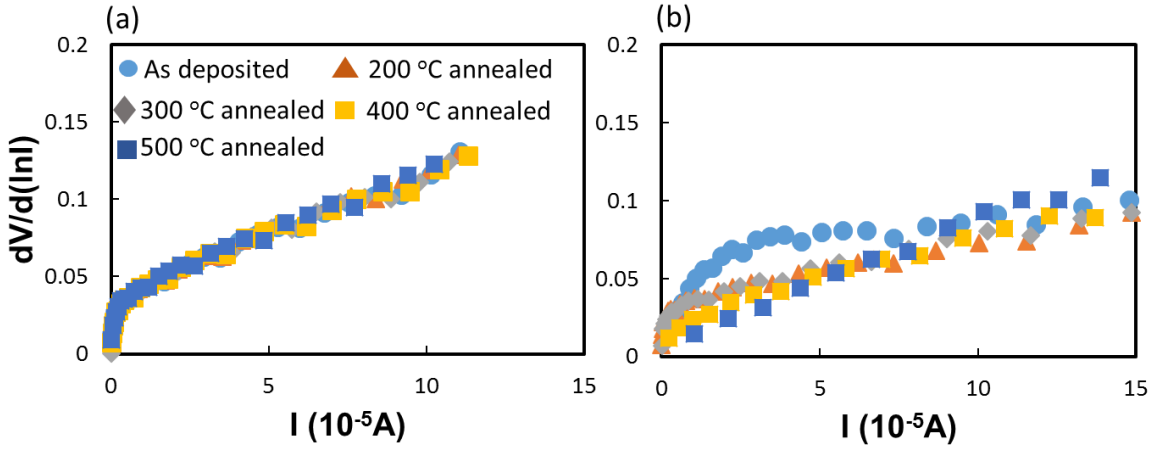

Figure 6.12. Plot of dV/d(InI) vs I of (a) MLG/n-GaN and (b) Ni/n-GaN diodes without annealing and after annealed at various temperatures ranging from 200 to 500 ºC.

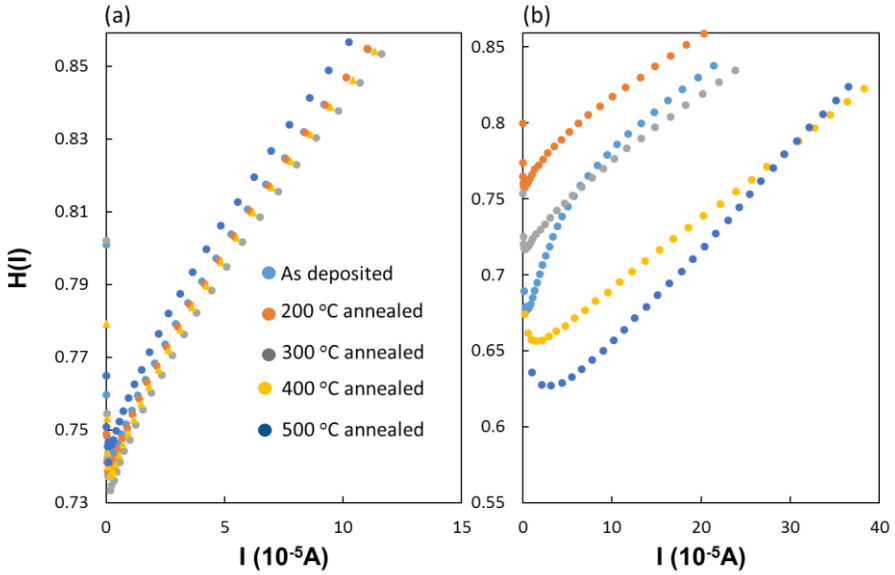

Figure 6.13. Plot of H(I) vs I of (a) MLG/n-GaN and (b) Ni/n-GaN diodes without annealing and after annealed at various temperatures ranging from 200 to 500 ºC.

to 500 ºC. R_s and SBH values were determined from slope and intercept of the curve after linear fitting of the curve. Figure 6.14 shows the variation of (a) SBH and (b) ideality factor derived by Cheung's method for MLG/n-GaN and Ni/n-GaN diodes without annealing and after annealed at 200 to 500 ºC. From Fig. 6.14(a), one can observe almost the same SBH variation for both diodes as was in case of TE model discussed above. Thus, the thermal

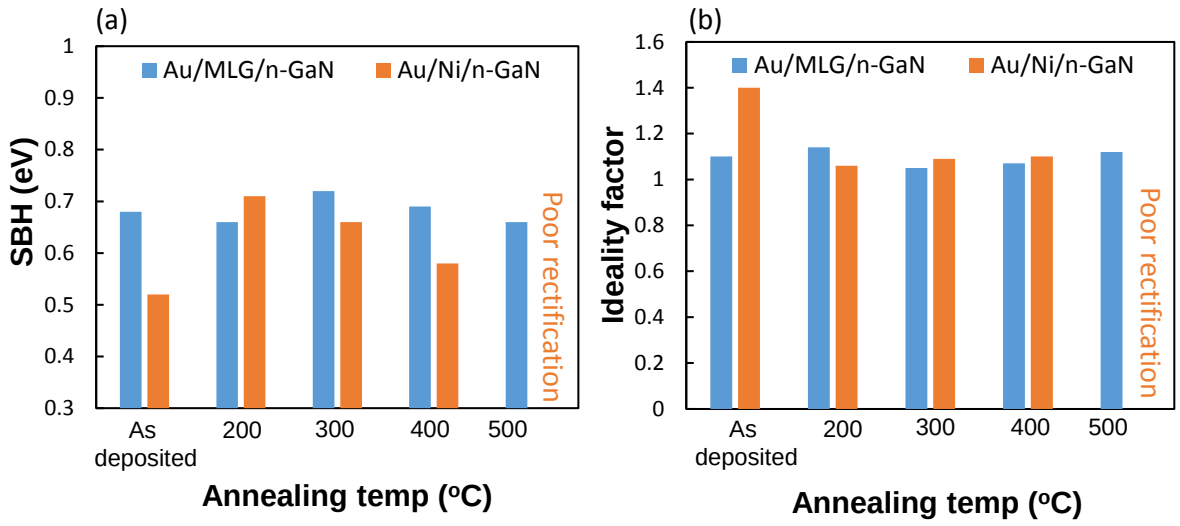

Figure 6.14. Comparison of (a) SBH and (b) Ideality factor of (a) MLG/n-GaN and (b) Ni/n-GaN diodes as measured by Cheung's function without annealing and after annealed at various temperatures ranging from 200 to 500 ^{o}C.

stability of MLG/n-GaN diode with small variation in SBH with annealing temperature was confirmed even if the diode properties were calculated by Cheung's method. One reason behind the thermal stability of MLG/n-GaN diode might be the surface reaction during the fabrication process of MLG. The surface reaction between n-GaN and MLG occurred at 650 ^{o}C during MLG fabrication. The maximum annealing temperature of 500 ^{o}C for determining thermal stability of the diode should not affect the surface reaction of the MLG/n-GaN diodes From Fig. 6.14(b), it is seen that the ideality factor values for both the diodes came close to unity when the calculation was carried out by Cheung's method which indicate we should take R_s into consideration while measuring the diode characteristics. Comparing the SBH of both the diodes, it was found that the SBH measured by TE model is little bit higher than those measured by Cheung's method but, the ideality factor measured by Cheung's method was closer to unity. Therefore, diode characteristics measured by Cheung's method is more accurate for our fabricated diodes.

6.5.3.3. Series resistance comparison of Au/MLG/n-GaN and Au/Ni/n-GaN diodes.

The R_s value of both the diodes were calculated using Cheungs function. To justify the accuracy of calculation of R_s, Norde method was also employed to calculate the series resistance of the fabricated diode. The calculation procedure of diode properties using Norde function is

described in Sect. 6.2.4. Figure 6.15 shows the variation of F(V) as a function of forward bias voltage for (a) MLG/n-GaN and (b) Ni/n-GaN diode without annealing and after annealed at

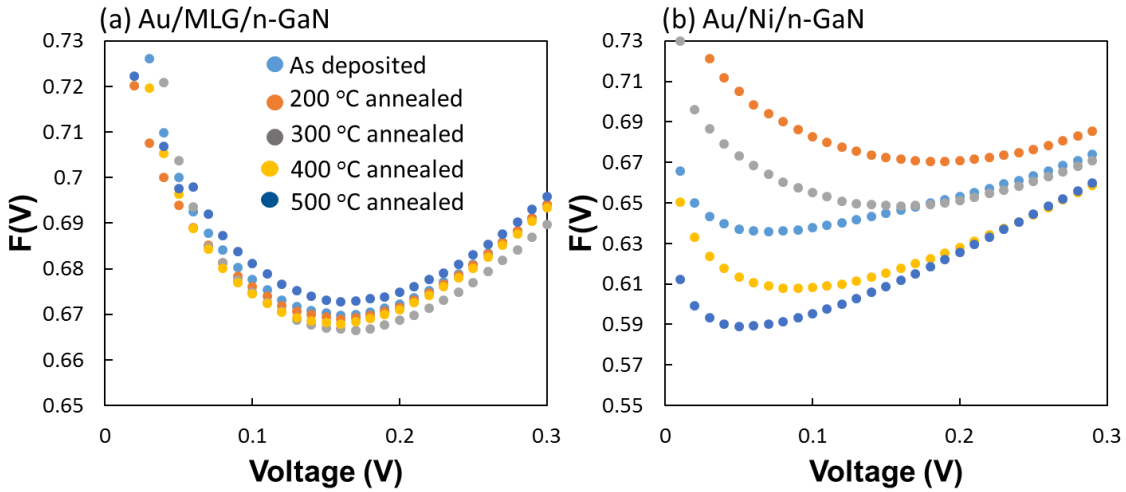

Figure 6.15. Plot of F(V) vs V of (a) MLG/n-GaN and (b) Ni/n-GaN diodes without annealing and after annealed at various temperatures ranging from 200 to 500 °C.

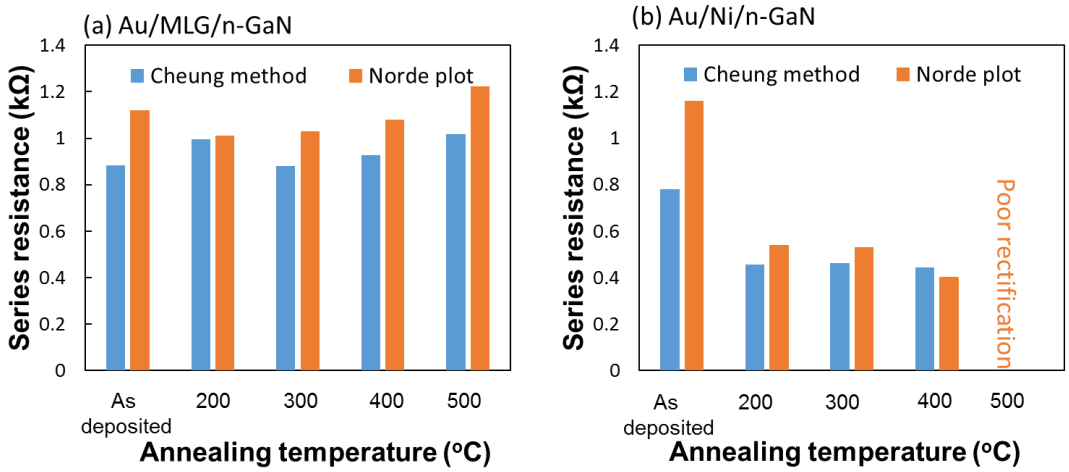

Figure 6.16. Comparison of series resistance as measured by Cheung's function and Norde plot for of (a) MLG/n-GaN and (b) Ni/n-GaN diodes without annealing and after annealed at various temperatures ranging from 200 to 500 °C.

various temperatures between 200 to 500 °C. The value of series resistance can be calculated by finding the minimum value of F(V) and using Eqn. 6.14.

Figure 6.16 shows the plot of series resistance as a function of annealing temperature for (a) MlG/n-GaN and (b) Ni/n-GaN diodes without annealing and after annealing at various

temperatures ranging from 200 to 500 ^{o}C measured by Norde function and Cheungs function. From the series resistance plot shown in Fig. 6.16, it is seen that the R_s values MLG/n-GaN diode is comparatively large in comparison with the Ni/n-GaN diodes. The high value of R_s for MLG/n-GaN diode might be due to the higher resistivity of MLG in comparison with Ni. The series resistance for MLG/n-GaN diode is almost constant with annealing temperature whereas decreasing with annealing temperature for Au/Ni/n-GaN diodes. It is also seen from Fig. 6.16 that the series resistance measured by Cheung's function and Norde plot are in good agreement with one another that confirms the accuracy of our calculation. It is seen from 6.16(b) that the series resistance of Au/Ni/n-GaN diode decreases after annealing. The reason behind the reduction of the series resistance of the Au/Ni/n-GaN diode after annealing in comparison with as deposited one is due to the crystallization of the Au particles after annealing as was confirmed from the XRD spectra of Fig. 6.18 later in this chapter.

6.5.3.4. Leakage current comparison of Au/MLG/n-GaN and Au/Ni/n-GaN diodes.

Figure 6.17 shows variation of leakage current as a function of reverse bias voltage for (a) MLG/n-GaN and (b) Ni/n-GaN diodes without annealing and after annealed at various temperatures ranging from 200 to 500 ^{o}C. From Fig. 6.17, it can be seen that the reverse leakage current of MLG/n-GaN diodes for annealing at and above 400 ^{o}C were smaller than the Ni/n-GaN diodes. Another important phenomenon for MLG/n-GaN diodes was that the reverse leakage current was almost independent of annealing temperature as can be seen from Fig. 6.17(a). The reason behind the small variation of leakage current of MLG/n-GaN diode is the

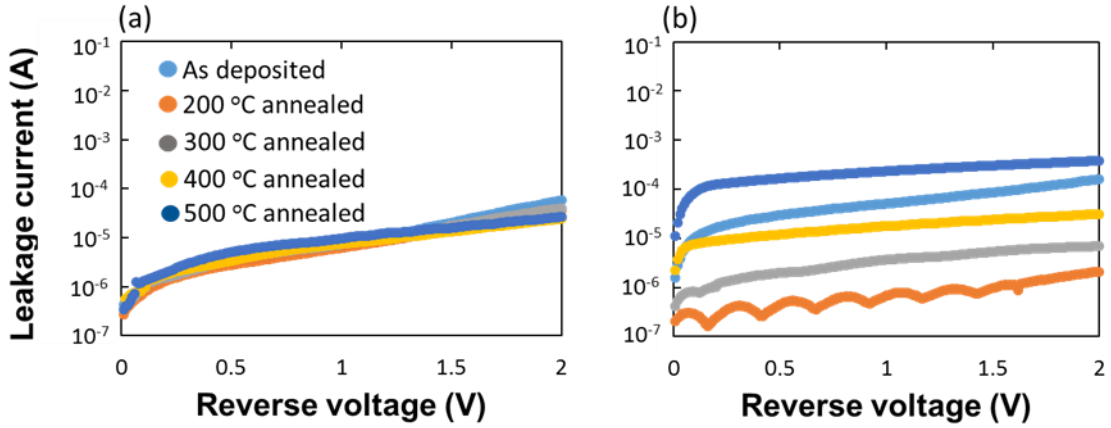

Figure 6.17. Comparison of leakage current as a function of reverse voltage for (a) MLG/n-GaN and (b) Ni/n-GaN without annealing and after annealed at various temperatures ranging from 200 to 500 ^{o}C.

almost stable SBH with respect to each annealing temperature.

From Fig. 6.17, it was found that the leakage current of our fabricated diode is larger. The reverse leakage current of a Schottky barrier diode (SBD) can be expressed as [32]

$$I_0 = J_{TE} + J_{GR} + J_S P \qquad (6.15)$$

Where, J_{TE} is the thermionic emission current density, J_{GR} is the generation-recombination current density, J_S is the surface leakage current density, and P is the perimeter of the device. It may be pointed out that the TE and GR currents are proportional to the area of the device, and hence J_{TE} and J_{GR} are defined as the leakage current components per unit area of the device with the dimension of A cm^{-2}. On the other hand, the surface leakage current is proportional to the perimeter of the device and J_S is defined as the surface leakage current per unit perimeter of the device with the dimension of A cm^{-1}.

Thus, the leakage current of a SBD is proportional to the area and perimeter of the Schottky contact. The area and perimeter of our fabricated device is larger in comparison with other reported literatures [5,6,26]. So, the increased leakage current of our fabricated diode is due to the larger area of the Schottky contact.

6.5.3.5. Interface reaction comparison of Au/MLG/n-GaN and Au/Ni/n-GaN diodes by XRD measurement.

To find out the interface reaction of the fabricated Au/MLG/n-GaN and Au/NI/n-GaN diodes, XRD measurements were carried out for as deposited diodes and after each annealing. Figure 6.18 shows the XRD spectra for (a) MLG/n-GaN and (b) Ni/n-GaN diodes without annealing and after annealed various temperatures between 200 and 500 ^oC. From the XRD spectra of MLG/n-GaN diode shown in Fig. 6.18(a), it is found that there is no interface reaction between Au and n-GaN as no compound phases were obtained in the XRD spectra for annealing the diode up to 500 ^oC. On the other hand, a compound $AuGa_2$ (511) phase was found to form for Ni/n-GaN diode when the diode was annealed at 400 and 500 ^oC as can be seen from Fig. 6.18(b). Sheu et al [33], investigated the structural properties of Ni/Au/GaN diode by X-ray diffraction measurements. They have identified that the formation of Au-Ga compounds due to high temperature annealing could reduce the barrier height, yielding a large reverse current. Our results are in accord with their report. The decrease of SBH and increase in reverse current of our Au/Ni/n-GaN diode might be due to the formation of Au gallide phase as shown in Fig. 6.18(b), after annealing at and above 400 ^oC. Since no gallide phases were found for MLG/n-GaN diode (XRD spectra of Fig. 6.18(a)) up to 500 ^oC annealing, the Au diffusion might be

stopped by MLG layer. It is reported that the MLG layer can be acted as a diffusion barrier layer against Au when the device is annealed at high temperatures [34].

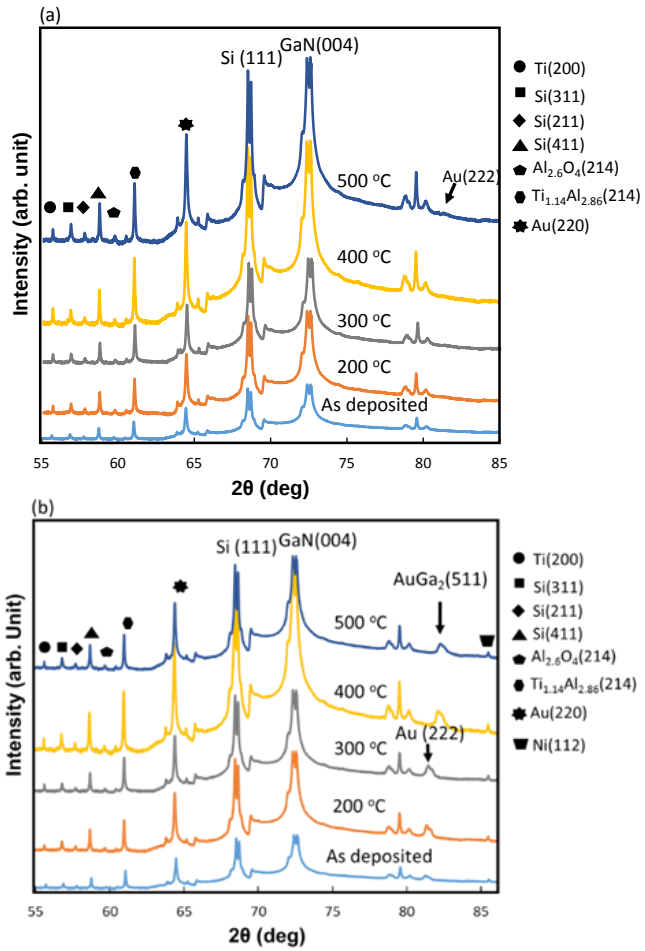

Figure 6.18. XRD spectra of (a) MLG/n-GaN and (b) Ni/n-GaN diodes without annealing and after annealed at various temperatures ranging from 200 to 500 ^{o}C.

6.6. Fabrication of a Cu/MLG/n-GaN SBD.

From the plotted results in Fig. 6.16, it was confirmed that the series resistance of MLG/n-GaN diodes were larger in comparison with those of Ni/n-GaN diodes. To reduce the series resistance of the MLG/n-GaN diodes, the top metal was changed from Au to Cu with the same thickness of 150 nm. Since the resistivity of Cu is smaller than Au, the series resistance of the MLG/n-GaN diodes should be reduced by changing the top metal to Cu. The top and cross sectional view of the fabricated diode is shown in Fig. 6.19.

The I-V characteristics comparison between Au/MLG/n-GaN and Cu/MLG/n-GaN diode is shown in Fig. 6.20. Both forward and reverse current of Cu/MLG/n-GaN diode is seen to be increased in comparison with Au/MLG/n-GaN diode. The SBH value of Cu/MLG/n-GaN diode was found to be 0.67 eV which is slightly smaller than the Au/MLG/n-GaN diode (0.72

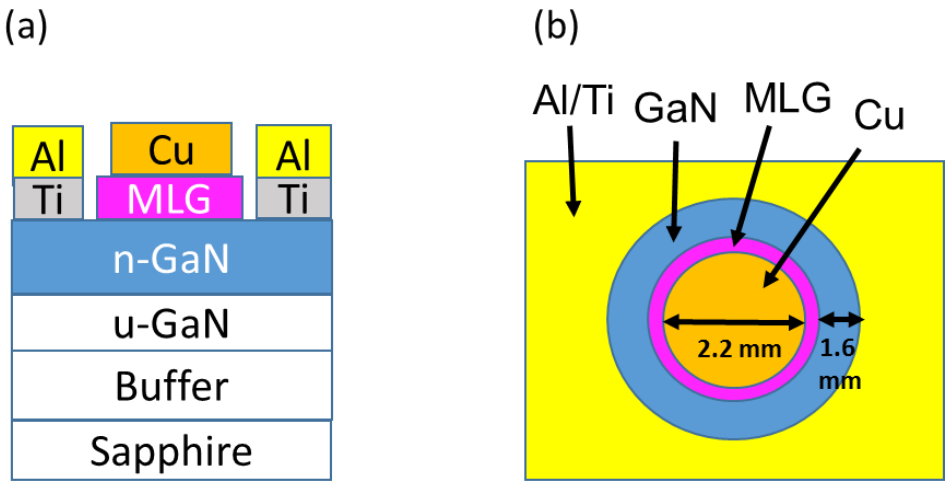

Figure 6.19. (a) Cross-sectional and (b) top view of Cu/MLG/n-GaN Schottky diode.

eV). The increase in reverse leakage current of Cu/MLG/n-GaN SBD should be due to the decrease in SBH values. The series resistance of Cu/MLG/n-GaN diode was found to be 0.88 kΩ which is slightly smaller than the Au/MLG/n-GaN diode (0.9 kΩ). The increase in forward current of Cu/MLG/n-GaN diode might be partially due to the decrease in series resistance in comparison with Au/MLG/n-GaN diode.

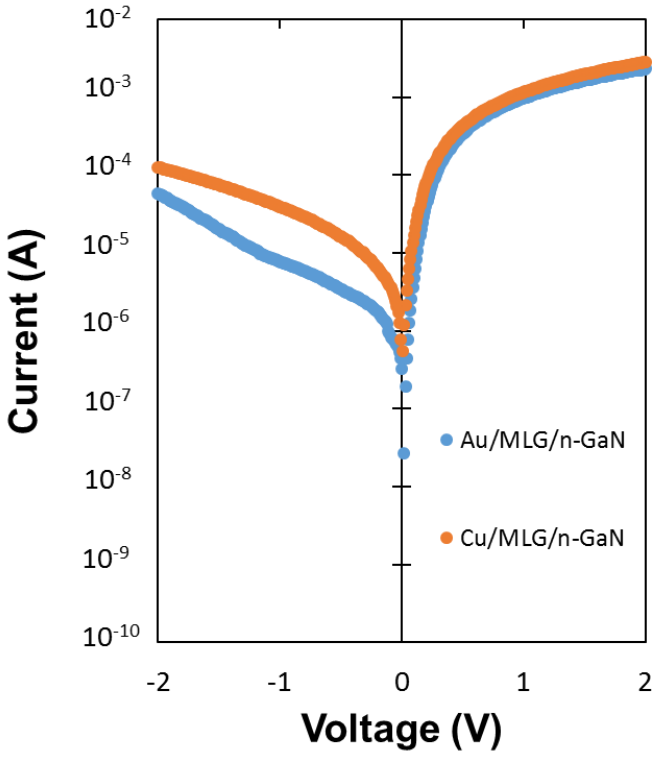

Figure 6.20. (a) I-V characteristics comparison between Au/MLG/n-GaN and Cu/MLG/n-GaN diodes.

Since, series resistance variation between Au/MLG/n-GaN and Cu/MLG/n-GaN is as small as 0.02 kΩ as mentioned earlier, therefore, the high series resistance comes from the contact resistivity of MLG and the top metal or the high resistivity of MLG.

6.7. Fabrication of MLG/n-GaN SBD changing the top metal from Au to Au/Ni.

From the plotted results and the previous discussion, it was found that the series resistance of the fabricated diode might be due to the high contact resistance of MLG and Au. To reduce the series resistance and to improve the forward bias I-V characteristics, we have fabricated SBD changing the top metal from Au to Au/Ni. It has been reported that the contact resistance of MLG with Ni is smaller than Au [35]. The fabrication process is shown in Fig. 6.21.

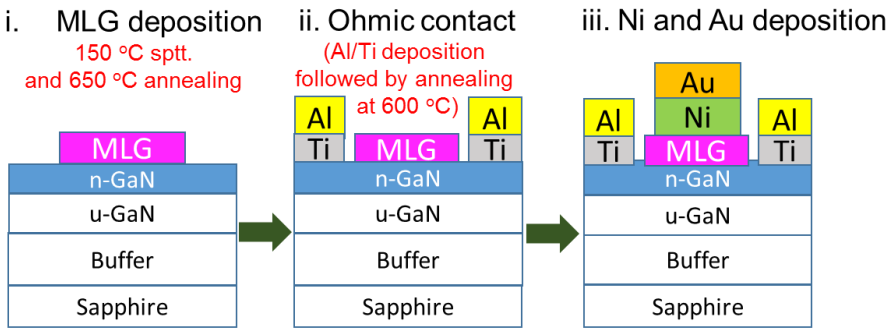

Figure 6.21. Process flow of fabrication of MLG/n-GaN diode with Au/Ni top contact.

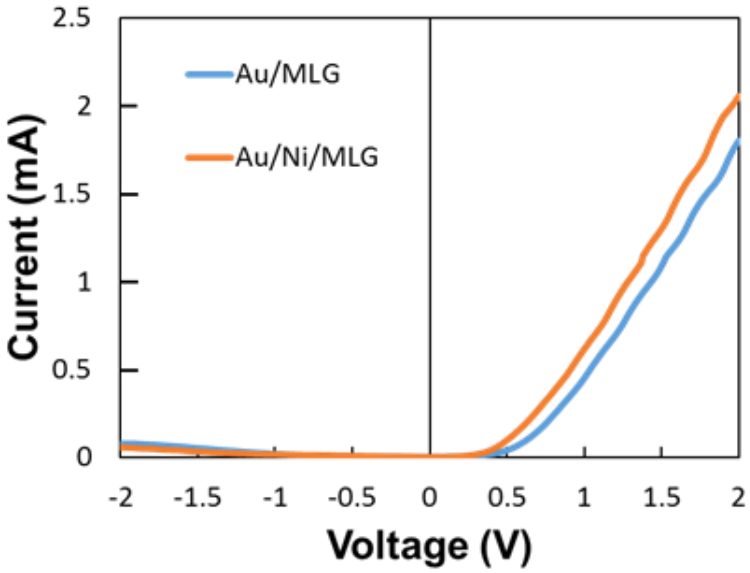

Figure 6.22. Comparison of I-V characteristics between Au/MLG/n-GaN and Au/Ni/MLG/n-GaN diodes.

Figure 6.22 shows the comparison of I-V characteristics of the fabricated Au/MLG/n-GaN and Au/Ni/MLG/n-GaN diodes. From Fig.1, it is seen that the forward bias I-V characteristics improved after changing the top metal from Au to Au/Ni. However, further work is required for the details.

6.8. Summary and conclusions

The fabrication and electrical characteristics of the MLG/n-GaN diodes have been reported by several research groups. Untill now the MLG based diodes are fabricated by transferring MLG from one substrate to another which is not ideal for many applications. In this context, we propose transfer-free deposition of MLG on n-GaN which has been described in the previous chapter. MLG/n-GaN diode is expected to have better thermal stability due to thermal structural stability of MLG. Although MLG/n-GaN diodes are being extensively studied, still there is a lack of studies on thermal stability of MLG/n-GaN diodes with transfer-free deposition of MLG. In this situation, we fabricated MLG/n-GaN diodes with transfer-free deposition of MLG on n-GaN by our new method. The findings of the current chapter can be summarized as follows

- The MLG/n-GaN diodes were fabricated with transfer-free deposition of MLG on n-GaN by solid-phase reaction with optimized deposition conditions as 150 ^{o}C sputtered Co/C layer annealed at 650 ^{o}C.
- The as deposited MLG/n-GaN diode showed rectification with a barrier height of 0.72 eV. The as deposited diodes SBH was found to be in good agreement with other available reported values.
- The thermal stability of the diodes were measured by measuring the I-V characteristics after annealing the diodes without annealing and after annealed at various temperatures ranging from 200 to 500 ^{o}C in vacuum of 5×10^{-3} Pa and was compared with a conventional Ni/n-GaN diode.
- It was found that the MLG/n-GaN diodes showed better thermal stability with more stable SBH than a conventional Ni/n-GaN diode annealing up to 500 ^{o}C. Moreover, the Au/Ni/n-GaN diode become ohmic after annealing at 500 ^{o}C but the Au/MLG/n-GaN diode shows rectification even annealing at 500 ^{o}C. The diode properties calculated by TE model and Cheung's method was found to be in good agreement with one another.
- From XRD measurement, no compound phases of GaN and Au was found after annealing the Au/MLG/n-GaN diode at 500 ^{o}C, whereas, a compound Au gallide phase was found after annealing the Au/Ni/n-GaN diode at 500 ^{o}C. That means, annealing up to 500 ^{o}C no reaction between Au and GaN occurred for Au/MLG/n-GaN diodes. On

the other hand surface reaction between Au and GaN occurred for Au/Ni/n-GaN diode.

- The unaffected interface reaction with annealing and the prevention of Au diffusion to n-GaN due to action of MLG as Au diffusion barrier layer is considered to be the reason behind the thermal stability as was confirmed by XRD measurements.
- The series resistance of MLG/n-GaN diode was found to be higher than the Ni/n-GaN diode.
- The Cu/MLG/n-GaN diode was fabricated by changing the top contact metal from Au to Cu. The series resistance change of the fabricated Cu/MLG/n-GaN diode was found to be negligible in comparison with Au/MLG/n-GaN diodes. Therefore, the high series resistance of MLG/n-GaN diode is considered due to the higher resistivity of the MLG layer or Au/MLG contact.
- The MLG/n-GaN diode was fabricated by changing the top metal from Au to Ni/Au and improvement of forward I-V characteristics was found. However, further work is needed for the details.

Our obtained results indicate that the MLG/n-GaN diode fabricated by our new method will be promising for improved thermal stability of n-GaN Schottky diodes in comparison with a conventional Ni/n-GaN SBD. However, the optimization of MLG thickness and reduction of series resistance will be required.

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CHAPTER SEVEN

CONCLUSIONS

7.1 Conclusion of each chapter

To fabricate multilayer graphene (MLG) with improved crystallinity and uniformity at lower temperature for interconnect and GaN based device applications, solid-phase reaction (SPR) method was studied in the present work. For the application of MLG, transfer-free deposition with improved crystallinity and uniformity is still a challenge. MLG fabrication by SPR has an advantage of transfer-free deposition onto the desired substrate. In this thesis, we have focused on the fabrication of MLG on SiO_2 and n-GaN substrate and application specially on n-GaN with improved crystallinity and uniformity by SPR. The conclusions described in this chapter cover the topics discussed from Chapter 3 to Chapter 6, as these chapters are the main contributions of this thesis.

7.1.1 Chapter 3

To fabricate MLG film directly with improved crystallinity and uniformity for interconnect application, a new approach of SPR with current stress application during annealing has been demonstrated. In this chapter, the effect of current stress during annealing on formation and crystallinity of MLG films by SPR have been studied. MLG films were fabricated directly on SiO_2 substrates by solid-phase precipitation with current stress application during annealing of a Co-C layer at a comparatively lower temperature. The effects of current stress on the formation and crystallinity of MLG films were investigated by comparing the characteristics of the films annealed at the same temperature with and without current by taking into account the temperature rise due to Joule heating. The characteristics obtained by Raman spectroscopy, scanning electron microscopy (SEM), transmission electron microscopy (TEM), and X-ray diffraction (XRD) measurements revealed that the MLG films produced were crystalline in nature. The MLG crystallinity as determined by G/D ratio was found to increase with applied current stress at the same temperature. From SEM observations, beside Joule heating, reduction of nucleation sites of MLG induced by current stress may be the potential reason for the improvement of the crystallinity of MLG films. From XRD measurement, the dominancy of fcc cobalt phase by applying current stress might be another reason behind improvement of crystallinity. We have also improved the uniformity of MLG films by depositing an additional

copper (Cu) capping layer over the Co-C layer. The additional Cu capping layer stops the Co agglomeration as Cu does not make alloy with Co at the deposition temperature that was used during the fabrication of MLG films. Finally we conclude, current stress application can lead to low-temperature fabrication of MLG with higher crystallinity by SPR.

7.1.2 Chapter 4

To fabricate MLG directly on n-GaN substrate for application in n-GaN based device, this chapter was focused on first attempt to fabricate transfer-free nanocarbon films on n-GaN by SPR by annealing sputtered a-C on n-GaN. Diamond like carbon films are found to form by annealing the a-C layer on n-GaN at temperatures between 800 and 1000 ^{o}C. The surface uniformity of the samples were seen to be improve with the increase of annealing temperature. Crystallization of a-C due to high temperature annealing or self-catalization of Ga due to breaking of GaN into Ga and N_2 at high temperature might be the reason behind DLC formation. However, by this method the nanocarbon crystallinity is poor and the fabrication temperature was high. For practical application, improvement of crystallinity and uniformity of the nanocarbon film and lowering of the deposition temperature are required and will be focused in the next chapter.

7.1.3 Chapter 5

To improve the crystallinity and to decrease the fabrication temperature, an additional Co layer were proposed as catalyst layer for SPR to occur. In this chapter, the transfer free fabrication of MLG films on n-GaN with improved crystallinity and uniformity with Co as catalyst has been demonstrated. After formation of MLG films, the Co layer will be removed. The MLG crystallinity were found to improve in comparison with available reports but the surface uniformity was poor. Due to annealing of the room temperature (RT) sputtered Co/C layer thermal expansion difference between GaN and Co/C occurred and the surface of th annealed film consisted of many hillocks as was confirmed by SEM photograph. The surface uniformity were improved significantly after applying heat sputtering for the deposition of amorphous C and Co layers. Decreasing the difference in the thermal expansion between GaN and Co/C, the suppression of the reaction between GaN and Co, and in situ cleaning of the GaN surface before sputtering might be the reasons for the improvement in the crystallinity and uniformity. The growth conditions for MLG with improved crystallinity and uniformity were optimized as follows: 150 ^{o}C sputtering of the Co/C layers annealed at 650 ^{o}C. Our method might be useful

for fabricating MLG-GaN device with transter-free deposition of MLG on n-GaN by solid-phase reaction as described in chapter 6.

7.1.4 Chapter 6

Au/MLG/n-GaN Schottky diodes were fabricated using our method described in chapter 5. The as deposited MLG/n-GaN diode showed rectification with a barrier height of 0.72 eV. The as deposited diodes SBH was found to be in good agreement with other available reported values. The thermal stability of the diodes were measured by measuring the I-V characteristics after annealing the diodes without annealing and after annealed at various temperatures ranging from 200 to 500 ^{o}C in vacuum of 5×10^{-3} Pa and was compared with a conventional Ni/n-GaN diode. It was confirmed that the MLG/n-GaN diodes showed better thermal stability with more stable SBH than a conventional Ni/n-GaN diode annealing up to 500 ^{o}C. It is reasonable that the MLG/n-GaN diodes have the thermal stability up to 500 ^{o}C because the MLG/n-GaN contact was formed at 650 ^{o}C annealing. The diode properties calculated by TE model and Cheung's method was found to be in good agreement with one another. The unaffected interface reaction with annealing and the prevention of Au diffusion to n-GaN due to action of MLG as Au diffusion barrier layer is considered to be the reason behind the thermal stability. However, the series resistance of MLG/n-GaN diode was found to be higher than the Ni/n-GaN diode. The Cu/MLG/n-GaN diode was fabricated by changing the top metal from Au to Cu. By comparing the series resistance of Au/MLG/n-GaN and Cu/MLG/n-GaN diode, it was found that the higher series resistance of the MLG/n-GaN diode is considered due to the higher resistivity of MLG. Reduction of series resistance will be necessary for future. Our obtained results indicate that the MLG/n-GaN diode fabricated by our new method will be promising for improved thermal stability of n-GaN Schottky diodes.

7.2 Overall conclusions

It can be concluded that the successful fabrication of transfer-free MLG films were demonstrated on SiO_2 as well as n-GaN substrate by SPR in present research work. The crystallinity and uniformity of MLG were improved significantly on both dielectric and n-GaN substrate. The fabrication temperature were also lowered. The deposited MLG films on n-GaN substrate were used to fabricate a SBD. The SBD fabricated by our proposed method showed rectification and better thermal stability than a conventional Ni/n-GaN SBD upto 500 ^{o}C annealing. Therefore, MLG fabrication by solid-phase reaction is considered to be a potential

method for fabricating transfer-free MLG films on both dielectric and GaN substrate with further process development.

Finally, it can be concluded that the implementation of our present work leads to fabricate high-performance and thermally stable GaN based Schottky diode and expected to increase the performance of electronic and optoelectronic devices that required thermally stable Schottky contact. The fabrication temperature has been reduced that will decrease the energy consumption from the conventional energy source during fabrication and leads to reduce the emission of greenhouse gases.

7.3 Suggestions for the future work

MLG is extensively studied for various applications including narrow interconnects, application as an active or passive layer in electronic and opto-electronic semiconductor devices owing to its outstanding physical and optical characteristics, including high intrinsic electron mobility, quantum electronic transport and good chemical and mechanical stability. Therefore, there are tremendous scopes to study of these materials in the view of scientific and technological worth. Hence to get the better performance for the devices with MLG deposited by SPR, the following research work may be extended:

1) To fabricate MLG interconnect with MLG deposited on SiO_2 by our proposed method with current stress by SPR.
2) To study effect of MLG thickness on the performance of the MLG/n-GaN SBD.
3) To optimize the MLG thickness for lowering the series resistance of MLG/n-GaN SBD
4) To find the minimum thickness of the MLG layer to be used as a diffusion barrier against Au.
5) Doping of MLG fabricated by SPR to reduce the series resistance of the fabricated MLG/n-GaN SBD.