METAL-INDUCED CRYSTALLIZATION OF GERMANIUM THIN FILMS

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A thesis submitted in fulfilment of
the requirements for the award of the degree of
Doctor of Philosophy

Functional Control Systems
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Declaration

I hereby declare that this dissertation or any part of this work are original and have not been submitted elsewhere for the award of other degree or any diploma.

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Acknowledgements

I would like to express the deepest appreciation to my advisor, Prof. Kentaro Kyuno, for his always support, help and guidance during all the time I was at Shibaura Institute of Technology (SIT). Not just only research works, the ideal for good living in Japan also given to me. There's no way it's going to be successful without guidance and suggestions from him, thank you again.

I would like to thank you my committee members Prof. Koji Kita (The University of Tokyo), Prof. Kazuyoshi Ueno (SIT), Prof. Kazuhiko Noda (SIT) and Prof. Masayuki Shimojo (SIT). Also, many thanks Dr. Hironori Seki (CSEF, SIT) for kindly supporting some of the experiments.

I would like to thank you SIT for providing the financial support for the doctoral program under Hybrid Twinning Program (HBT) scholarship. My three years as a PhD. student at SIT has been an honor and pride for me and my family. I had a lot of good opportunities to study, to do research and have good experiences with new friends. It is an incredible journey in my life.

Finally, I gratefully acknowledge my parents and friends for always being encouraging to me.

Narin Sunthornpan

Abstract

Germanium (Ge) is one of the most intensively studied semiconductor materials because of its superior properties, such as higher carrier mobility and smaller energy bandgap compared to silicon (Si). These properties are advantageous in applications such as thin-film transistors, solar cells, next generation MOSFETs, etc. Nevertheless, because of its higher cost, fabricating high quality crystalline Ge thin films is a key to realizing these devices. Moreover, it would be advantageous if the low-temperature process is developed to fabricate these films on glass and plastic films. Metal-induced crystallization (MIC) technique is a rapidly emerging technique because it can crystallize Ge films at temperatures much lower than other methods like solid phase crystallization (SPC). Moreover, the method is simple and more suitable for large area processing compared to the laser annealing process. In MIC, to decrease the crystallization temperature, the introduction of metal layers such as aluminum (Al), silver (Ag) and gold (Au) is required as catalysts. Especially by using Au as a metal catalyst, the crystallization of amorphous Ge (a-Ge) films can be realized at a lower temperature (<300°C), which is low enough to fabricate high-quality crystalline Ge (c-Ge) thin films on plastic substrates such as polyimide films.

In the MIC method, an a-Ge/Au bilayer is annealed to crystallize the a-Ge layer. During the process, the Ge and Au layers exchange their positions. In most studies, a thin oxide layer is inserted between the a-Ge and Au layers to promote layer exchange. Nevertheless, this insert layer suppresses interlayer diffusion and a long annealing time, ~100 hours, is necessary. To solve this problem, the crystallization mechanism of Ge in the Au-induced crystallization method without an insert layer has been examined in this thesis. It is found that a layer exchange crystallization occurs even without an insert layer. The crystallization mechanism is clarified, and it is shown that by optimizing the process, it is possible to obtain a continuous c-Ge film with a smooth surface by annealing at 170°C for 1 hour. These findings will be useful for the fabrication of high-quality Ge thin films on various inexpensive flexible substrates which can be used as seeding layers for next generation solar cell application.

In chapter 1, the history of the MIC process is reviewed, and the aim of the thesis is explained.

In chapter 2, experimental methods adopted in the present study is introduced together with their operation mechanisms.

In chapter 3, we investigated the crystallization behavior of Ge thin films by Au catalysts without an insert layer. By annealing an a-Ge/Au bilayer up to 220°C, it is found that a layer-exchange type crystallization of Ge is possible even without an insert layer. As for the Au thickness dependence, it is found that the best Ge crystallinity is achieved with an initial Au layer as thin as 9 nm. This behavior seems to be brought about by the substrate which promotes heterogeneous nucleation of crystalline Ge. A higher (111) orientation is also realized for thinner Au samples. These findings are encouraging in terms of the smaller consumption of rare metals like Au.

The effect of initial a-Ge layer thickness on the crystallization behavior is also examined. It is found that the initial a-Ge layer thickness affects the morphology of the resulting c-Ge thin films. A double c-Ge layer structure has been confirmed. The bottom c-Ge layer has a thickness close to the original Au layer and has a better crystal quality compared to the top c-Ge layer. This morphology resembles that of crystalline semiconductor thin films obtained by annealing Al/Si and Al/Ge systems. It is possible to control the surface coverage of these layers by adjusting the initial Au and a-Ge thicknesses. Nearly 97% of the substrate surface is covered by the bottom c-Ge layer with a small amount of top c-Ge layer by annealing an a-Ge(46nm)/Au(29nm) bilayer at 220°C. The resulting ~30nm thick Ge film shows a hole mobility of as high as ~85 cm^2/Vs reflecting a high coverage.

In chapter 4, the crystallization mechanism without an insert layer has been investigated in detail. The results show that the Ge atom diffuse from the a-Ge layer into the Au layer and nucleation of c-Ge occurs inside the Au layer. Lateral growth of c-Ge proceeds by the Ge supply through the Au layer. This explains why the bottom c-Ge layer has a same thickness as the original Au layer. As the c-Ge layer grows on the substrate, Au is pushed up to the top layer and layer exchange completes. The top c-Ge layer starts to nucleate at a higher temperature compared to the bottom layer. A poor crystal quality implies a different growth mechanism for the top layer. A small amount of Au diffused into the a-Ge layer could have crystallized Ge without layer exchange.

In chapter 5, the findings in chapters 3 and 4 have been utilized to develop an efficient process to obtain a continuous c-Ge layer with a small surface roughness at low

temperature. In chapter 4, it is found that the top layer starts to nucleate at a higher temperature compared to the bottom layer. This implies that by annealing at a low temperature for a certain period of time, it might be possible to increase the coverage of the bottom layer while suppressing the nucleation of the top layer. By annealing an optimized thickness bilayer, a-Ge(46nm)/Au(29nm), at 220°C with a heating rate of 0.5°C/min, the coverage of as high as ~99% for the bottom c-Ge layer with a small amount of top layer has been obtained. This result supports the assumption that it is possible to grow only the first layer by adjusting the bilayer thickness and annealing at a low temperature for a certain period of time, which is enough to complete the bottom layer. Moreover, to obtain a (111) oriented film, a thinner bilayer, a-Ge(18nm)/Au(10nm) has been adopted. By annealing this bilayer at 170°C for 1 hour, a highly (111) oriented c-Ge layer has been obtained with a small amount of top layer.

Chapter 6 includes the summary of the thesis and future prospects.

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International Journal

1. **N. Sunthornpan**, K. Kimura and K. Kyuno, Morphology of Ge thin films crystallized by Au-induced layer exchange at low temperature (220°C), Journal of Vacuum Science and Technology B, **40** (2022) 030601.
2. **N. Sunthornpan**, K. Kimura and K. Kyuno, Crystallization of Ge thin films by Au-induced layer exchange: effect of Au layer thickness on Ge crystal orientation, Japanese Journal of Applied Physics, **61** (2022) SB1029.
3. **N. Sunthornpan**, K. Tauchi, N. Tezuka and K. Kyuno, Effect of gold layer thickness on the low-temperature crystallization process of germanium thin films by gold-induced crystallization, Japanese Journal of Applied Physics, **59** (2020) 080904.

International conference

1. **N. Sunthornpan**, and K. Kyuno, "Realizing an atomically flat surface of Ge (111) thin film at low temperature (220°C) by gold-induced layer exchange", The 64th Electronic Materials Conference (EMC 2022), June 29-July 1, 2022.
2. **N. Sunthornpan**, N. Tezuka, K. Kimura and K. Kyuno, "In-situ observation of low-temperature crystallization process of germanium thin films by gold-induced layer exchange", The 8th International Symposium on Organic and Inorganic Electronic Materials and Related Nanotechnologies (EM-NANO 2021), June 1-3, 2021.
3. **N. Sunthornpan**, K. Kimura and K. Kyuno, "Controlling the Morphology of Ge Thin Films Crystallized by Gold-Induced Layer Exchange at Low Temperature (220°C)", International Conference on Solid State Devices and Materials (SSDM 2021), September 6-9, 2021.
4. **N. Sunthornpan**, K. Kimura and K. Kyuno, "Influence of Gold Layer Thickness on the Metal-Induced Crystallization Behavior of Ge Thin Films", The 67th American Vacuum Society Symposium (AVS 67), October 25-28, 2021.
5. **N. Sunthornpan**, K. Kimura and K. Kyuno, "Low Temperature Crystallization of Ge Thin Films for Channel Layers of Thin-Film Transistors by Gold-Induced Layer Exchange", Materials Research Society Fall Meeting & Exhibit (MRS 2021), December 6-8, 2021.

Domestic conference

1. **N. Sunthornpan** and K. Kyuno, "Metal-Induced Crystallization Process of Ge thin films", 1st Green Electronics Symposium (IRCGE 1st), February 25, 2022.

Chapter 1

Introduction

1.1 Overview

This chapter describes the research background, including the history of the metal-induced crystallization (MIC) technique, problems, and critical issues. The motivations for this thesis are also included. Chapter also reviews the research related to the MIC technique. The research objectives are outlined, and some possible device applications are explained.

1.2 Motivations

Electronic devices play an important role in daily life. Smartphones, radios, televisions, laptops, video games, and advanced medical diagnostic equipment would be unavailable without them, and semiconductors are important integral components of these electronic devices. Semiconductor materials used for integrated circuits or microchips are composed of pure elements, such as silicon (Si) or germanium (Ge), as well as compounds like gallium arsenide (GaAs). Among the group IV elements, Si is the most common semiconductor material in various electronic devices because of its low-cost and easy to acquire. Ge is recognized as a next-generation semiconductor material for electronic device applications because of its higher carrier mobility, lower bandgap and better lattice matching with III-V compound semiconductors than Si [1, 2]. Ge is used for the bottom layers of multijunction solar cells to increase the IR absorption efficiency [3-5]. However, these applications use single crystalline or epitaxial Ge, which is unsuitable for large-scale production. Therefore, it is necessary to develop a more cost-efficient process.

In nanotechnology, thin films are superior to bulk semiconductor materials because they enable the low-cost production of semiconductor devices over a large area with the desired geometry and structure. In particular, thin-film semiconductors on low-cost flexible substrates are promising for developing highly efficient semiconductors for modern electronic devices. In addition to low cost, the advantages of flexible electronics include interfacial conformability, bendability, stretchability, and lightweight [6]. Thin-film semiconductors on flexible substrates are also used for flexible electronics and have attracted increasing attention recently because they provide many novel applications concerning multiple areas, such as flexible circuits [7, 8], implantable medical devices [9], flexible displays [10-15], electronic textiles [16], electronic paper [17, 18], wearable devices [16, 19, 20], conformable radio frequency identification devices [21-23], and electronic skin for robots [24-26]. However, the limited process operating temperature range is the main challenge of using inexpensive flexible substrates.

The deposition of high-quality Ge thin films on flexible substrates requires the crystallization temperature to be as low as possible while maintaining the quality. Several processes have been developed to crystallize Ge films, such as solid phase crystallization (SPC), which can crystallize Ge films at ~500°C [27, 28]. Metal-imprint-induced crystallization techniques have been studied to realize the crystallization of Ge films at

several annealing temperatures (315°C-625°C) [29, 30]. Laser annealing was also used to crystallize Ge films, enabling a small crystallization area and long crystal grains (>100μm) with a low thermal budget [31]. However, these techniques require much higher crystallization temperatures than the working temperature of flexible substrates, which should be lower than 300°C.

Recently, MIC techniques have been studied extensively because they can crystallize Ge films at temperatures much lower than other methods like SPC [28, 32]. Moreover, the MIC method is simple and more suitable for large area processing than the laser annealing process [33, 34]. In MIC, the introduction of metal layers, such as aluminum (Al), silver (Ag), and gold (Au), is required as catalysts to decrease the crystallization temperature [32, 35, 36]. In particular, using Au as a metal catalyst, the crystallization temperature of amorphous Ge (a-Ge) films can be lower than 300°C, which is low enough to fabricate high-quality crystalline Ge (c-Ge) thin films on many plastic substrates, such as polyimide films.

The MIC technique can be applied to crystallize high-quality Ge thin films on inexpensive flexible substrates at low temperatures for modern electronic device applications. The MIC process with Au as a catalyst was reported to realize poly-Ge at lower temperatures than other metal catalysts. An interfacial diffusion-limiting layer (oxide insert layer) is introduced between the metal and semiconductor interface to limit the diffusion of semiconductor atoms into the metal layer, which promotes layer exchange and the formation of a continuous c-Ge layer. However, a very long annealing time (20-250 h) is required because of the insert layer [37, 38]. Moreover, an additional step is required to remove the oxide layer, which is usually performed using a wet etching process. The etching solution (an aqueous HF solution) could also react with the crystalline semiconductor layer and etch some parts of the crystal [36]. Therefore, it is ideal if a complete layer exchange is possible without an insert layer by controlling the crystallization process in the MIC method.

1.3 Research objectives

- To develop an efficient process to realize high-quality Ge thin films using Au-induced crystallization without an insert layer.
- Examine the crystallization process without an insert layer to understand the crystallization mechanism.

1.4 Crystallization of Ge thin films using the MIC technique

1.4.1 History of the MIC technique

Among the various methods for crystallizing amorphous semiconductor thin films, such as Si and Ge, MIC is one of the most promising techniques for realizing high-quality crystalline semiconductor thin films. This is due to the lower crystallization temperature of MIC than that of other techniques such as SPC methods. Moreover, the MIC is more easily applicable to large area processing than laser annealing.

Oki et al. [39] reported MIC in 1969. They achieved the crystallization of a-Ge at low temperatures when it was in contact with metals, such as Al, Ag, Au, Cu, or Sn. Bosnell and Voisey found that amorphous Si could also crystallize at low temperatures when placed in contact with a metal [40]. The vacuum evaporation technique was used to fabricate amorphous semiconductor films. Herd et al. [41] and Ottaviani et al. [42, 43] examined these effects using electron microscopy. This phenomenon is called metal-contact-induced crystallization [41]. They reported that the MIC process involves the mixing of semiconductors and metals, which results in the formation of small crystals of Si or Ge inside the metal [41-43]. In the 1990s, in situ transmission electron microscopy (TEM) was performed to examine the MIC process of layered structures of simple eutectic systems, such as Al/a-Si, Ag/a-Ge, and Ag/a-Si [44-48].

The MIC process has been discussed theoretically on the basis of thermodynamics and kinetics [49-63], which highlighted the importance of the interface. Auger electron spectroscopy depth profiles have also been applied to examine the kinetics involved in the MIC process in terms of the diffusion kinetics in metal/semiconductor layered systems [49, 51, 56]. More recently, in situ TEM has been used to examine the atomistic mechanism of the MIC process [64, 65].

1.4.2 Mechanisms of MIC

Figure 1.1 presents a diagram of the generally accepted mechanism of the layer exchange MIC. At the initial state, the amorphous semiconductor diffuses into the metal catalyst (Fig. 1.1(a)). Diffusion is believed to occur mainly at the grain boundaries in the metal layer. The concentration of semiconductor elements increases and supersaturates in the metal layer, which promotes the amorphous semiconductor to nucleate inside the metal layer (Fig. 1.1(b)). The semiconductor atoms diffuse through the metal layer, which leads to the growth of a crystalline semiconductor. The lateral growth of the crystalline semiconductor causes the metal to be pushed up to the top layer (Fig. 1.1(c)). Eventually, a crystalline semiconductor forms a bottom layer, and metal forms an upper layer to complete the layer exchange (Fig. 1.1(d)) [35,66-70].

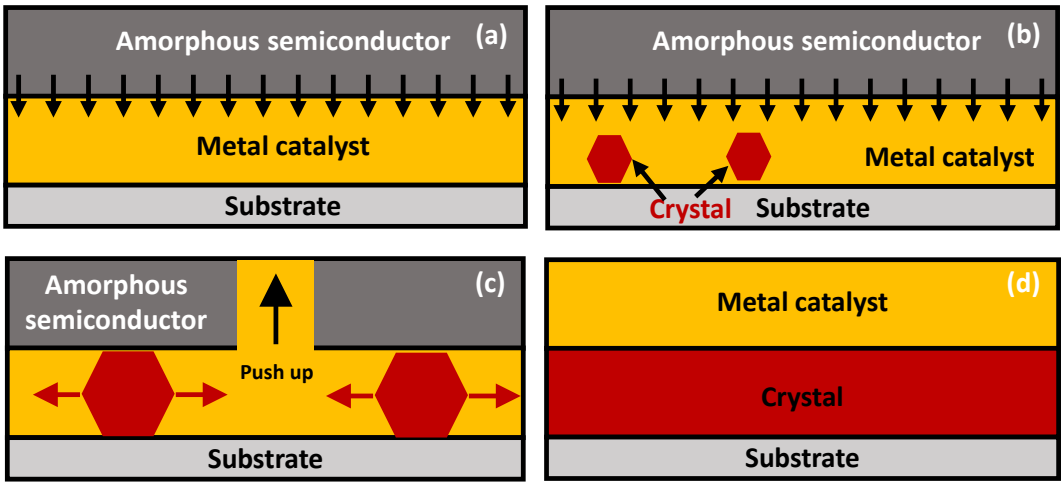

Fig. 1.1. Schematic of the layer exchange process. (a) Diffusion of semiconductor atoms from the amorphous layer into the metal layer. (b) Nucleation of crystalline semiconductor in metal. (c) Lateral growth of crystalline semiconductor and metal push up. (d) Completion of layer exchange.

1.5 Crystallization of Ge thin films by MIC using an insert layer

A crystallization method has been developed to achieve layer exchange in the MIC process by inserting an appropriate interlayer between the metal and semiconductor for a long time. These studies are summarized in Table I.

Table I. Summary of studies on MIC with insertion layer.

Year	Author	Type of film	Type of insert layer	Summary
1977	Harris et al. [70]	Al-Si	Native SiO_2	Inclusion of a native oxide (SiO_2) layer between the deposited Si and Al layers greatly retarded the crystallization process.
1996	Kim et al. [71]	Al-Si	Native SiO_2	Al-induced crystallization of the a-Si thin film occurred by interdiffusion of Al and Si atoms through the native oxide layer at the interface. The crystallization phenomena take place within or near the native SiO_2 layer during the annealing process.
2000	Nast et al. [72]	Al-Si	Native AlO_x	Thicker native oxides promote the growth of larger isolated grains. Continuous crystalline layer is achieved by increasing the annealing time.
2005	Barghouti et al. [73]	Al-a-Si:H	Native SiO_2	The crystallization rate of a-Si:H is considerably lower in the presence of a native oxide. Larger grains were obtained when an appropriate thickness of native oxide (~1.5 nm) was used. Moreover, the sample crystallized with a native oxide had a smoother surface than the sample without an oxide layer.
2009	Kurosawa et al. [74]	Al-$Si_{1-x}Ge_x$	Al_2O_3	Studied the effects of interfacial oxide layers on the Al-induced crystallization (AIC) of amorphous $Si_{1-x}Ge_x$ (x: 0-1). It was

Year	Author	Type of film	Type of insert layer	Summary
				found that the interfacial oxide layers were necessary to obtain large polycrystalline Si grains (~100 μm) with (111) orientation. However, in the case of SiGe, the interfacial oxide layers significantly retarded AIC growth. Consequently, layer exchange occurred inhomogeneously, which resulted in inhomogeneous crystallization even after a long annealing time (410ºC, 100 h). To solve this problem, complete layer exchange was achieved by controlling the air exposure time (oxide layer thickness). The appropriate air exposure time is shown in Fig. 1.2.
2009	Kurosawa et al. [75]	Al-Si	Al_2O_3	Studied the control of the crystal orientation of Si film on insulating substrate by MIC. They developed the interfacial-oxide layer modulated Al-induced low temperature (<450°C) crystallization technique, which realizes (001) or (111) oriented Si films with large grains (20–100μm). The thicker Al_2O_3 layers led to larger grain size and (111) orientation. These results are qualitatively explained based on the phase transition of the interfacial Al oxide layers.
2012	Okada et al. [76]	Al-Si	SiO_2	They fabricated poly-Si thin films on fused silica substrates by the Al-induced crystallization (AIC) method with SiO_2 insertion layers with different thicknesses (0-20nm). The morphologies the Si films

Year	Author	Type of film	Type of insert layer	Summary
				depend on the thickness of insert layer. Thin layer (2nm) realized high growth rate with (100) orientation, while thick layer (10nm) realized low growth rate with (111) orientation. These results imply that the crystal orientation depends on the diffusion rate of Si atoms into the Al layer.
2012	Toko et al. [77]	Al-Ge	AlO_x	They investigated the effect of annealing temperature and thickness of insertion layer by controlling the air exposure time. The fraction of (111) orientation reached 99% by combining the low-temperature annealing (325ºC) with the appropriate thickness of native oxide (AlO_x) diffusion control layer. The results are summarized in Fig. 1.3. The results are explained by the low interfacial energy of the (111) plane. The low annealing temperature and thick native oxide realized the low-diffusion rate of Ge and Al atoms. These make it difficult to generate the other planes with high-interfacial energies.
2012	Park et al. [78]	Au-Ge	Al_2O_3	Thin Al_2O_3 layers were inserted between Au and a-Ge layers to control crystal nucleation. (111) oriented large Ge grains (< 20 μm) were obtained at 350ºC by optimizing the interfacial oxide layer thickness. This result is attributed to the suppression of random bulk nucleation of Ge in Au films and the promotion of interfacial nucleation at Ge/SiO_2 interfaces.

Year	Author	Type of film	Type of insert layer	Summary
2013	Nakazawa et al. [79]	Al-Ge	AlO_x	Formation of large Ge grains by Al-induced layer exchange by adjusting the Ge/Al thickness. With an appropriate Al and Ge layer thickness, high coverage of the bottom-Ge layers and suppression of the nucleation of the top-Ge layers are realized. The fraction of (111) orientation reached 97% and the average grain diameter was 70μm.
2014	Toko et al. [80]	Al-Ge	AlO_x	The Al-induced crystallization (AIC) yields a large-grained (111)-oriented Ge thin film on an insulator at temperatures as low as 180ºC. They accelerated the AIC of an amorphous Ge layer (50 nm thickness) by doping Al in Ge, which facilitates Ge diffusion into Al. The electron backscatter diffraction measurement demonstrated the simultaneous achievement of large grains over 10μm and a high (111) orientation fraction of 90% in the polycrystalline Ge layer formed at 180ºC.
2014	Numata et al. [81]	Al-Ge	AlO_x + Ge membrane	They investigated the effects of Ge insertion below the Al layer. The Ge insertion layer promoted AIC by enhancing supersaturation of the Ge in Al, which resulted in low-temperature growth (275°C). However, thick (≥3 nm) Ge insertion layers provided a high nucleation rate and a small grain size. A use of 1 nm thick Ge insertion layer resulted in large grains of over 100μm in diameter.

Year	Author	Type of film	Type of insert layer	Summary
				Moreover, the film was highly (111) oriented.
2015	Higashi et al. [82]	Au-Ge	Al_2O_3	A modulated Au-induced layer exchange crystallization method with an atomic-layer deposited Al_2O_3 barrier and a-Ge/Au multilayers is established. Large (~600μm) and (111)-oriented pseudo-single-crystalline Ge grains are realized at 275°C. The crystallinity was better than Ge layers obtained by Al-induced technique.
2017	Yoshimine et al. [83]	Ag-Ge	SiO_2	Investigation of Ag-induced layer exchange (SILE) of a-Ge on insulators including a plastic substrate. Although layer exchange between Ag and Ge was difficult because of the high diffusion rate of Ag into Ge, they achieved the complete layer exchange by controlling the annealing temperature. The SILE led to the crystallization of a-Ge at 250ºC, allowing for the direct synthesis of crystalline Ge on a plastic substrate. Low temperature growth is attributed to the high solubility of Ge in Ag at low temperatures. This study proposes the importance of the solubility of semiconductors in metals and the diffusion coefficients of metals in semiconductors to realize layer exchange.
2021	Singh et al. [36]	Au-Ge	GeO_x	Introduction of GeO_x layer at Au/Ge interface for crystallization of Ge films. Polycrystalline Ge thin films were realized on glass substrates using Au-induced layer

Year	Author	Type of film	Type of insert layer	Summary
				exchange crystallization process at ~170ºC. The role of the interfaces, particularly grain boundaries of Au in enabling the crystallization much below the bulk crystallization temperature is discussed. The acceptor states introduced by point defects lead to p-type semiconducting behavior in the thin film with a low resistivity ~1Ω cm at room temperature. While the grain boundary scattering mechanism limits the carrier conduction, the hole mobility of ~50 cm^2/Vs at 300 K is the highest among poly-Ge thin films formed at such a low temperature (170ºC or lower).

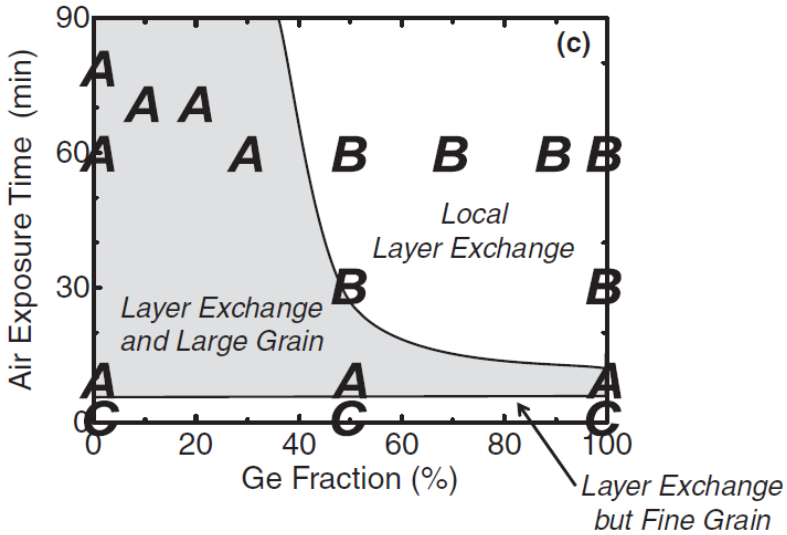

Fig. 1.2. Summary of growth features depending on air exposure time and Ge fraction [74]

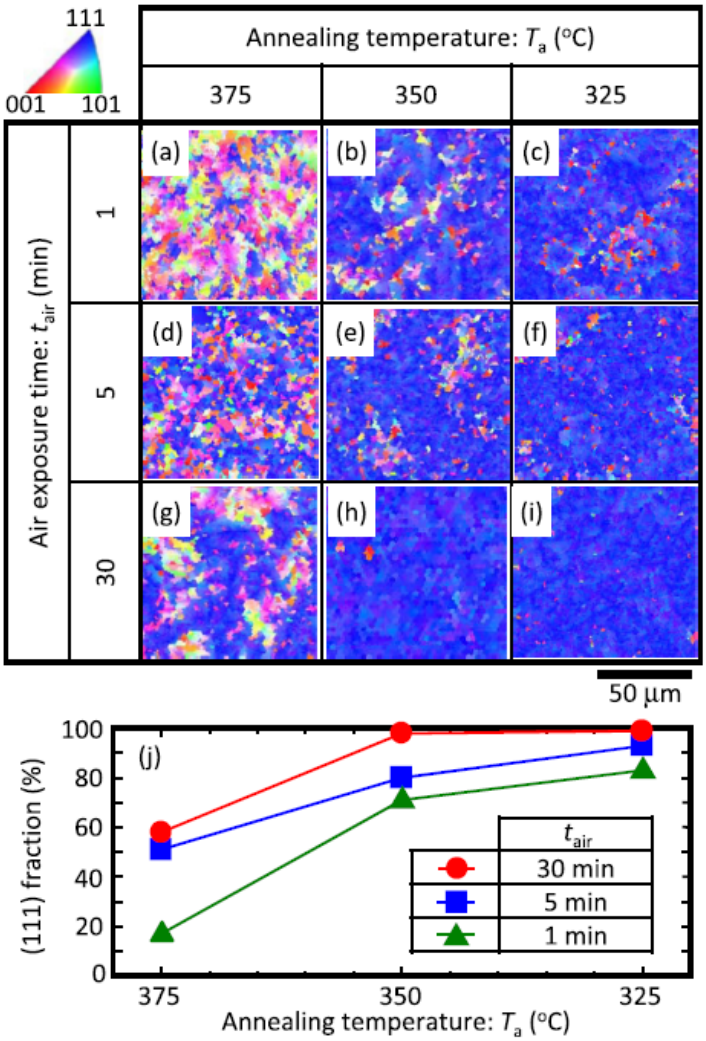

Fig. 1.3. The orientation of c-Ge films as a function of insert layer thickness and annealing temperature [77].

Harris et al. [70] reported that the native SiO_2 between the a-Si and Al layers retarded the crystallization process. Kim et al. [71] examined the crystallization of a-Si by Al with a native SiO_2 insert layer at the atomic level by cross-section TEM. Al induced the crystallization of a-Si thin films by the interdiffusion of Al and Si atoms through the native oxide layer. The crystallization behavior was explained on the basis of diffusion, which occurs within or near the native SiO_2 layer during the annealing process, as shown in Fig. 1.4 [71].

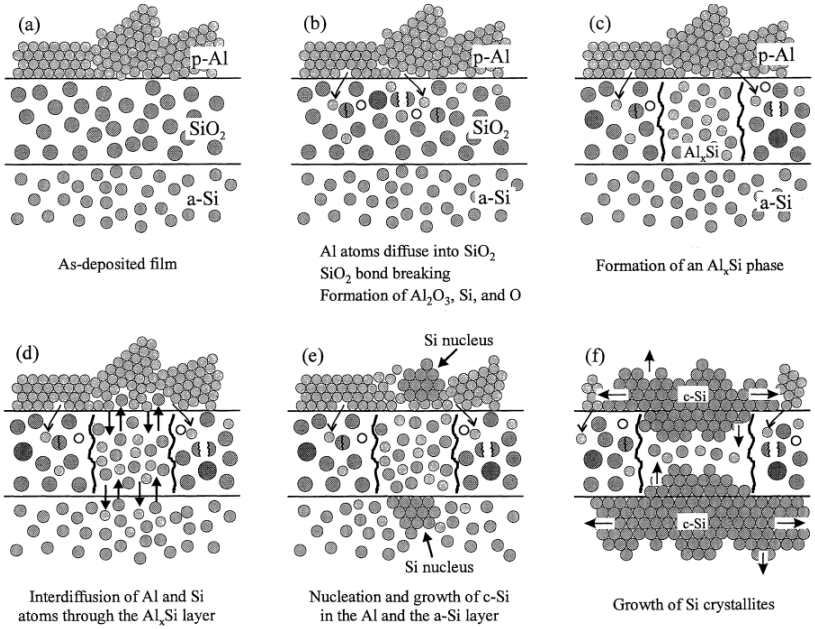

Fig. 1.4. Schematics of the crystallization mechanism of Al/SiO_2/a-Si structure [71].

The layer exchange model was developed to achieve a continuous c-Si layer, which is formed at the original position of the metal (Al) sublayer at low temperatures even without the introduction of the insert layer [56, 57, 66, 67, 84, 85]. According to the layer exchange mechanism, the following conditions must be considered for layer exchange to occur: (i) the semiconductor dissolves well in the metal, (ii) the semiconductor and metal do not form compounds and (iii) the semiconductor diffuses into the metal before the metal diffuses into the semiconductor. Conditions (i) and (ii) can be examined from the phase diagram [67, 68]. It is a convenient guide to finding the material combination for layer exchange. Although condition (iii) is difficult to evaluate because of the lack of data, it is possible to control the diffusion rate and achieve layer exchange by inserting an appropriate interlayer between the metal and semiconductor [83]. The quality of the metal and amorphous semiconductor layers, which varies according to the preparation method and conditions, also affects the layer exchange process [86-89]. The effects of the native oxide layer thickness on crystallization have been studied [37, 78]. A large grain with a (111) orientation was obtained by optimizing the interfacial oxide layer thickness. The larger grain size contributes to higher carrier mobility because the amount of grain boundary is reduced. Park et al. [38] fabricated a high-carrier-mobility Ge film on flexible substrates by Au-induced crystallization with an oxide layer. The hole mobility was as high as 160 cm^2/Vs. Figure 1.5 [37] shows the

effect of the insertion layer thickness on the crystal orientation. The (111) orientation is realized when c-Ge nucleates on the SiO_2 surface.

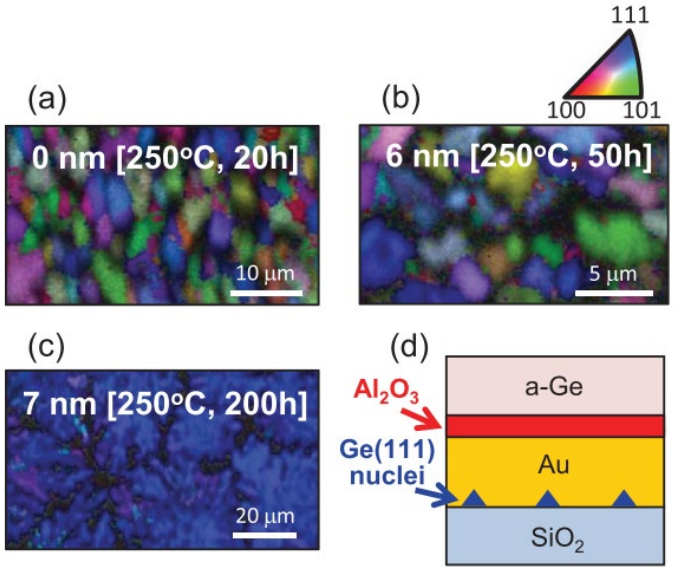

Fig. 1.5. EBSD images of Ge layers grown on quartz substrates [interface layer thickness: (a) 0 nm, (b) 6 nm, and (c) 7 nm], and schematic explanation of (111)-oriented nucleation on SiO_2 (d). The annealing conditions are shown in the EBSD images. [37]

The introduction of an appropriate insert oxide layer is useful for achieving layer exchange, large grain formation and control of the crystal orientation. However, it requires a very long annealing time and high temperatures because the insert layer acts as a barrier to limit the diffusion of semiconductor atoms into the metal layer. Moreover, as in the case of the AlO_x insert layer in the growth of c-Ge by Au-induced crystallization, an additional step is needed to remove the AlO_x layer using an aqueous HF solution in addition to removing the top Au layer using KI and I_2 solution. There is a possibility that any residual AlO_x during etching may affect the properties of poly-Ge thin films. Moreover, a part of the poly-Ge thin film formed by MIC may also be etched away or destroyed by the aqueous HF solution because of the high reactivity of Ge to etching agents [90]. Because of these concerns, it is essential to produce Ge thin films using a Au-induced process without an interfacial insert layer.

1.6 Device applications of semiconductor thin films crystallized by MIC

1.6.1 Solar cells

Crystalline Si films fabricated by MIC have been applied to solar cells because Al-induced crystallization can produce large grain sizes [90]. The low-temperature crystallization process of MIC is advantageous for depositing thin film semiconductors on low-cost substrates, such as glass or plastics. The epitaxial growth of Si on large grain p-type Si formed by Al-induced layer exchange has been studied [91-93]. Additionally, epitaxial thickening of Si on the seed layer has been performed using various techniques, such as ion-assisted deposition [94, 95], CVD [94-101], and solid-phase epitaxy [102-104]. Nevertheless, the conversion efficiency needs to be improved by improving the quality of c-Si [90]. Additionally, the invert layer exchange has been examined because it can provide a self-organized Al bottom electrode [105].

The seed layer formation of the Ge layer crystallized by Al has been well studied. Using Ge thin films instead of a bulk Ge substrate in multijunction solar cells is attractive because of the cost reduction and light absorption efficiency. A Ge thin film grown epitaxially on a large-grain p-type Ge seed layer formed by the MIC with an Al catalyst exhibited a bulk minority carrier lifetime of 5.6μs, which is close to that grown on a single-crystal Ge [106]. The Ge also provides a good lattice matching with group III–V compound semiconductors. A GaAs pseudo single crystal (grain size >100μm) with high (111) orientation has been grown on a Ge thin film fabricated using an Al-induced MIC technique [107]. The photoresponsivity property of GaAs film on Al-induced Ge film was close to that of the GaAs film on a single-crystal Ge wafer.

1.6.2 Thin-film transistor

Thin-film transistors were also fabricated in which Ge thin films crystallized using the MIC technique were used as channel layers [108, 109]. Metal catalysts, such as Au and Ag, were used [110, 111]. Low contamination of Au and Ag is expected in Ge grown by Au and Ag catalysts because of their low solid solubility in Ge [32]. The Hall effect mobility as high as 210 cm^2/Vs has been reported for Ge thin films crystallized by Au-induced crystallization because of the large Ge grain size successfully developed at low crystallization temperatures (<300°C) [32, 35]. Moreover, transistor operation was

obtained using the pseudo single crystal Ge layer formed on glass and plastic substrates [32, 112]. Field-effect mobility as high as 70 and 10 cm^2/Vs is achieved on glass and plastic substrates, respectively. The decrease in leakage current remains a problem. The formation of n-type Ge thin films by the Ag-Sb catalysts at low temperature (330°C) has also been reported [111]. This opens up the possibility of fabricating complementary metal-oxide-semiconductor devices on flexible substrates.

1.6.3 Thermoelectric generator

Although Si–Ge alloys are very useful as thermoelectric materials [113], the process of bulk Si-Ge formation by sintering is expensive. Si–Ge alloy films can be produced using many techniques, such as sputtering [114], CVD [115, 116], SPC [117], and MIC [118]. A high-temperature process is required to achieve a high-power factor in Si-Ge for thermoelectric generators, particularly for improving the electrical conductivity by dopant activation. However, the MIC technique can provide Si-Ge films with high electrical conductivity even at low crystallization temperatures by impurity doping. Hence, the MIC using Al or Zn as metal catalysts to produce p-type Si–Ge achieved a high-power factor with a low-temperature process [119, 120]. Moreover, high performance on flexible substrates was also achieved. An excellent power factor of 240 $\mu W/mK^2$ was obtained using a $Si_{0.4}Ge_{0.6}$ layer fabricated on a polyimide substrate from MIC with Al-induced crystallization, which is very useful for environmentally friendly inorganic semiconductors formed on flexible plastic substrates [121]. The conduction type of the Si-Ge film can be adjusted to n-type using Ag or Au as the metal catalysts and initially doping them with n-type impurities. As a result, the layer exchange approach is promising for developing Si–Ge films that may be used to fabricate highly reliable flexible thermoelectric generators.

1.6.4 Rechargeable batteries

Significant progress has been made in the development of thin-film rechargeable batteries for next-generation mobile devices or sensors [122]. New techniques are required to produce anode, solid electrolyte, and cathode materials on various substrates. Graphite, an anode material for common rechargeable batteries, cannot be synthesized directly on most substrates because the synthesis temperature is too high (~3000°C). The

inverted layer exchange, however, allowed self-organization of the anode electrode structure, which is a graphite thin film (MLG) on a current collector metal at low temperatures (~600°C) [123]. An identical structure was constructed on a Mo substrate to analyze the anode performance, which acted as a Li-ion battery anode. Si and Ge are also considered anode materials because of their high capacity [124]. A Li-ion battery with excellent anode characteristics of 1650 mAh/g after 500 cycles has been demonstrated by the formation of a nanostructured Si anode with a large surface area using the layer exchange technique [125]. These findings will open up the possibility of developing flexible rechargeable batteries because group IV materials are useful as anodes and can be fabricated on various plastic substrates using the MIC technique.

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Chapter 2

Experimental

2.1 Overview

This chapter describes the details of substrate preparation and film deposition method which has been performed by RF magnetron sputtering technique. Crystallization process of Ge thin film is performed by MIC technique with annealing process under N_2 atmosphere. Structural characterization of Ge thin films was performed using X-ray diffraction (XRD), Raman spectroscopy, electron backscatter diffraction (EBSD) and transmission electron microscope (TEM). Surface morphology has been investigated with the help of scanning electron microscopy (SEM) and atomic force microscope (AFM). The electrical properties of Ge thin films were also characterized by Hall effect measurement. Thin-film transistor was fabricated by using the crystallized Ge film as a channel layer and the operation has been successfully demonstrated.

2.2 Film fabrication

2.2.1 Substrate

A Si wafer with a 100 nm thermally grown oxide layer (SiO_2/Si) was used as substrate for this experiment. Prior to film deposition, samples were cleaned to remove the organic and inorganic contamination by acetone and ethanol using an ultrasonic cleaning bath for 20 min each and dried with N_2 gas.

2.2.2 Film deposition

The RF magnetron sputtering was used to fabricate Au/Ge bilayers. RF magnetron sputtering can deposit thin films on both conductive and insulating substrates. The schematic diagram of the RF magnetron sputtering system is shown in Fig. 2.1. This sputtering system can hold up to three targets at once, making it possible to fabricate bilayers without breaking high vacuum. The substrates can be rotated to position them over the next target, and different layers can be deposited successively under high vacuum. Prior to the sputtering process, the chamber was pumped to high vacuum around 1.6×10^{-2} and 1.6×10^{-6} Torr by using rotary and cryogenic pumps, respectively. The deposition of Au (Au target: 99.99%) and Ge (Ge target: 99.999%) was performed by RF magnetron sputtering process with high-purity Ar (99.9999%) gas plasma with substrates at room temperature (Ar gas flow: 10 ccm, pressure: 3×10^{-3} Torr). The sputtering condition are shown in Table II.

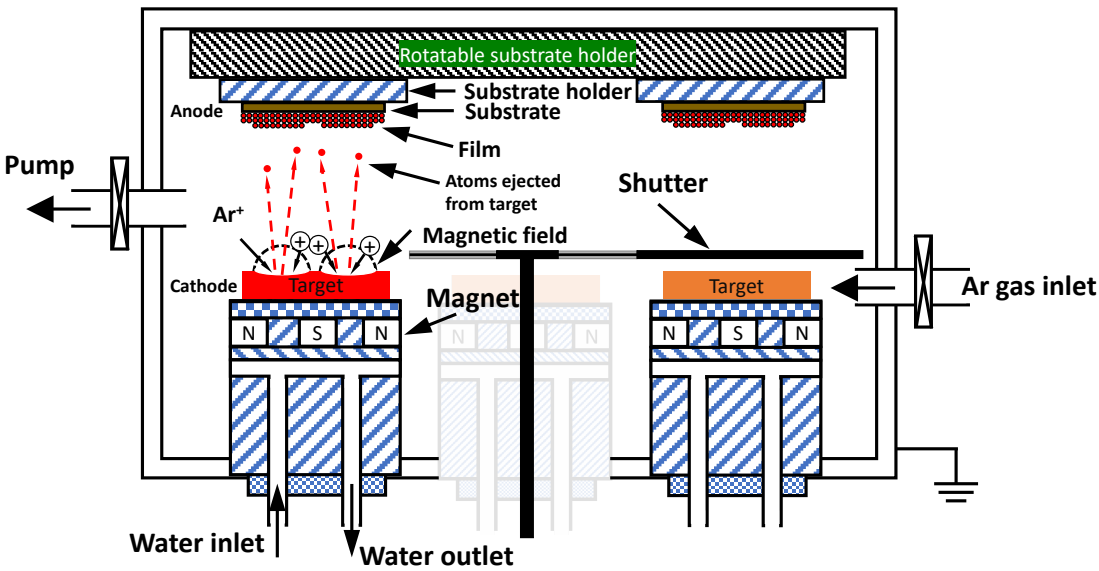

Fig. 2.1. Schematic of RF magnetron sputtering.

Table II. Deposition condition of Au and Ge films by RF magnetron sputtering.

Films	Pressure (Torr)	RF power(W)	Ar flow rate (ccm)	Film growth rate (nm/sec)
Au	3×10^{-3}	100	10	0.72
Ge	3×10^{-3}	70	10	0.33

2.3 Experimental methods for investigating the MIC process

2.3.1 X-ray diffraction (XRD)

X-ray diffraction (XRD) is one of the most useful techniques for analyzing the occurrence and kinetics of a phase transformation process, such as crystallization [1]. The emergence and increase of the intensities of related diffraction maxima provide crucial information on the (initial) nucleation and (subsequent) growth of a certain crystalline semiconductor phase. This method can be applied to both bulk specimens and thin films and does not require any additional specimen preparation procedure.

In the XRD system, X-ray diffractometers include an X-ray tube, sample holder and X-ray detector. In a cathode tube, X-rays are generated by bombarding electrons created by heating a filament with a target while applying a voltage. Characteristic X-rays are created. The detector is spun constantly, and the intensity of diffracted X-rays is recorded. Based on the crystal structure and lattice constants, the pattern is material intrinsic, generating peaks of differing intensities at various angles (θ). Bragg's law is used to explain the relationship as shown in equation 2.1 and schematic views of X-ray diffraction are given in Fig. 2.2.

$$n\lambda = 2d\sin\theta \tag{2.1}$$

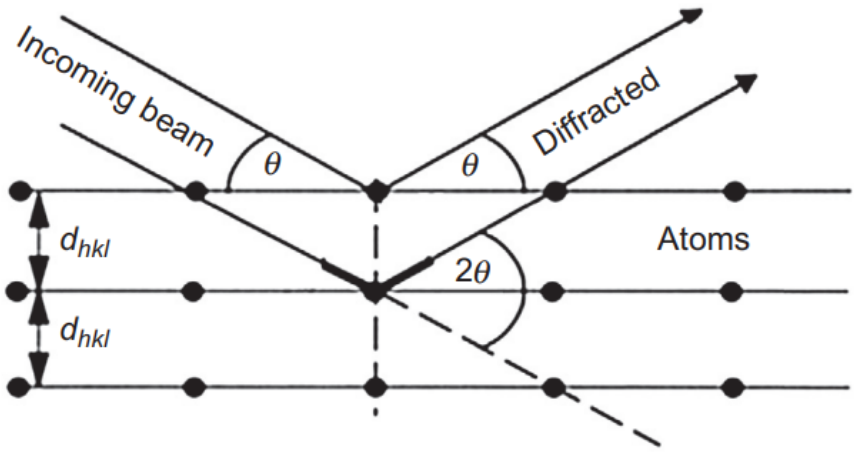

Fig. 2.2. Geometrical condition for diffraction from lattice planes [2].

The X-ray beam at certain angles (θ) reflects at the cleavage faces of the crystal. λ is the beam wavelength. The variable *d* is the distance between atomic layers in the crystal, *n* is an integer. Typically, the material is clarified by comparison of *d*-spacing with standard patterns on standard peak databases of each material [3, 4]. To examine the kinetics of MIC processes, in-situ XRD experiments has been performed with a heating stage under nitrogen atmosphere [1, 3, 5].

However, the very initial stage (nucleation) in the crystallization process is not detected by XRD, because a minimum crystalline phase is required to generate a detectable diffraction signal. As a result, the amount of crystallization temperatures determined by in-situ XRD are frequently slightly higher than those determined by other techniques such as TEM or Raman measurement, and can thus be considered as an upper limit for the crystallization temperatures. The X-ray diffractometer was set to 40 kV and 15 mA with Cu-Kα radiation, and λ = 1.5404 was obtained.

2.3.2 Raman spectroscopy

Raman spectroscopy is a useful method for quickly determining the vibrational energy modes of molecules. It is based on photon scattering that is inelastic. Photon scattering is induced when laser light interacts with molecular vibrations, and the energy levels of the scattered photons are shifted up or down.

As shown in Fig. 2.3, changes in the energy levels of scattered photons provide information about the vibrational modes.

The incident photons are referred to as "elastic or Rayleigh scattering." Raman scattering is an inelastic scattering phenomenon that involves the transfer of energy between a molecule and a scattered photon. If the molecule acquires energy from the scattered photon, it will have less energy than the incoming photon, resulting in a longer wavelength (Stokes). However, if the scattered photon receives energy from molecules, the fianl energy level is lower than the initial state, and the wavelength of the scattered photon is shorter (Anti-Stokes). The Stokes and anti-Stokes lines have the same frequency range. The Stokes shift is commonly observed using Raman measurements.

In this experiment, Raman spectroscopy was used to investigate the crystal quality of Ge thin film. The peak observed around 300 cm^{-1} corresponds to crystalline Ge. The 532-nm laser excitation with a 2.5% ND filter was used for this measurement.

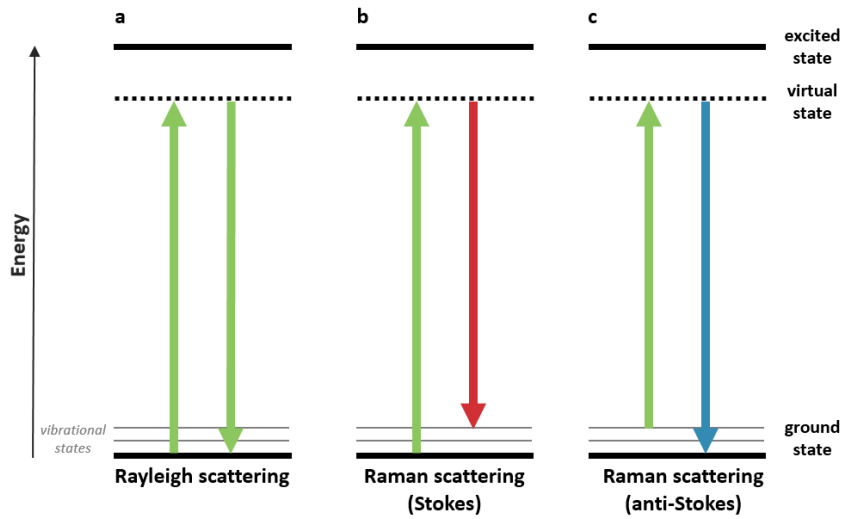

Fig. 2.3. Schematic diagram of the energy transitions involved in Rayleigh and Raman scattering (Stokes and anti-Stokes lines) [6].

2.3.3 Scanning electron microscopy (SEM) and energy dispersive X-ray (EDX) analysis

Scanning electron microscopy (SEM) is one of the most powerful equipment to investigate surface morphology. Secondary electrons are emitted from the surface of a sample when it is bombarded with an electron beam. The surface morphology can be observed by scanning an electron beam over the surface in two dimensions and detecting secondary electrons. Figure 2.4 depicts the basic configuration of a SEM [7]. An electron gun, condenser lens, and objective lens are required for the SEM. The scanning coil is used to move the electron beam along the x- or y-axis over the sample surface. The secondary electrons generated from the sample surface are detected using secondary electron detectors. The secondary electrons are collected to create a picture. A high vacuum of 10^{-3}–10^{-4} Pa must be maintained inside the chamber.

Energy dispersive X-ray (EDX), equipped with SEM, is a technique to identify chemical composition of materials. This is a function of obtaining a spectrum of the energy intensity of X-rays using a combination of semiconductor detector and spectrum analyzer.

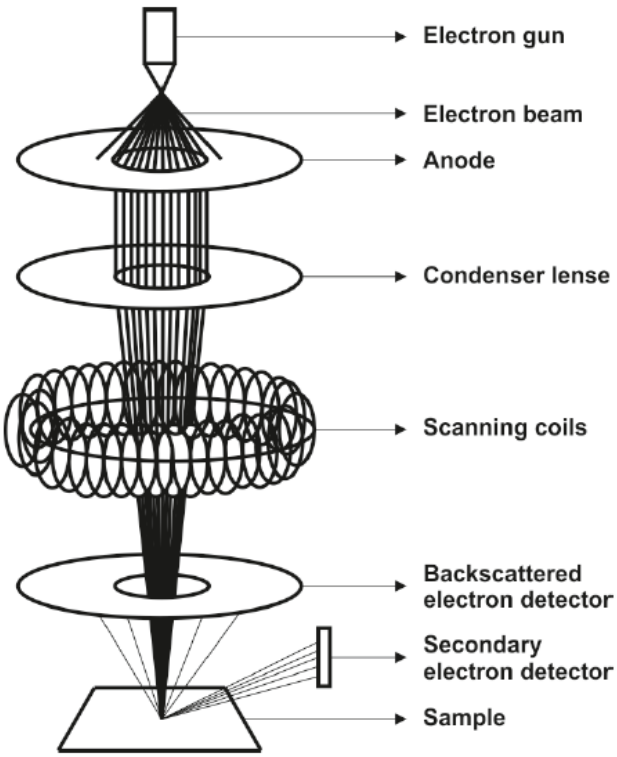

Fig. 2.4. Schematic representation of a SEM setup [8].

2.3.4 Transmission electron microscopy (TEM)

Transmission electron microscopy (TEM) is one of the most advanced techniques to observe the microscopic feature of a material. A beam of electrons is sent through a specimen to generate an image in TEM. As seen in Fig. 2.5 [9], electrons interact intensively with atoms via elastic and inelastic scattering. As a result, the specimen must be very thin to allow electrons to pass through it, roughly 5-100 nm for a 100 keV electron beam. The thickness of the sample is determined by the specimen's density and elemental composition. The use of elastic scattering of electrons in a highly localized location allows for very high resolution. Electrons scattered inelastically are not localized. Because of interactions with nuclei's electrostatic potential, the electron beam trajectory shifts slightly during elastic scattering. The entire electron beam returns to the detector to generate the image since there is no significant momentum loss. The energy of electrons in the beam is transferred to the specimen in an inelastic collision, inducing diverse effects including excitation, ionization, and lattice vibrations [10].

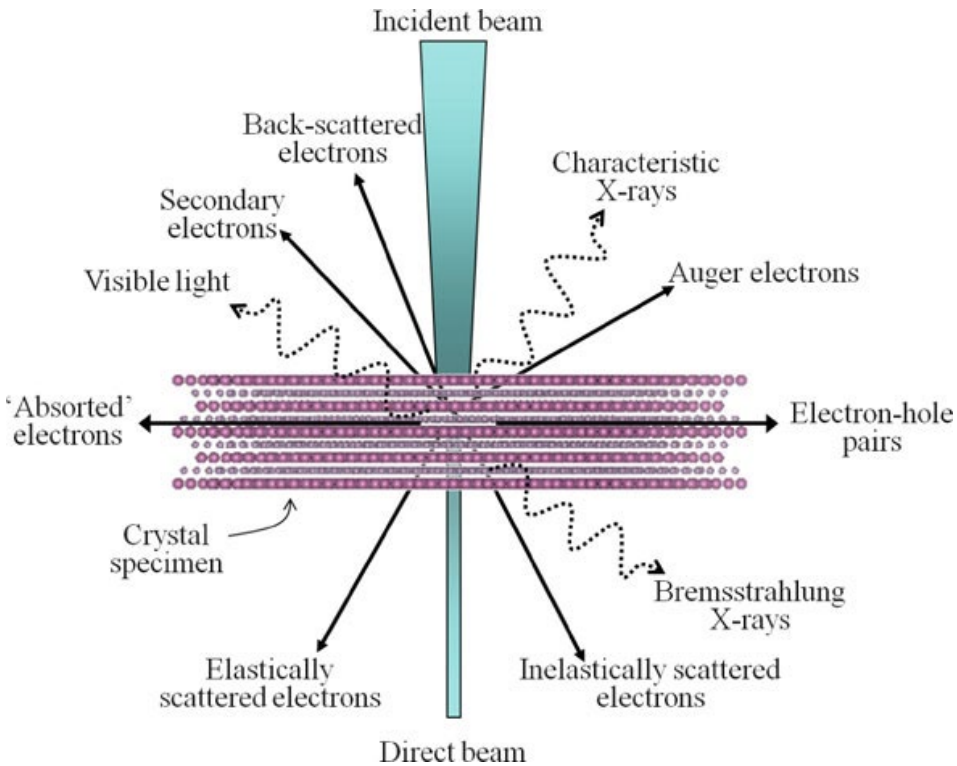

Fig. 2.5. Signals generated from the interaction between a high energy electron beam and an electron transparent (very thin) sample [9].

The highly localized and ultra-high magnification images with high resolution in the crystallization process can be provided by TEM technique. Thus, the very initial stage in the crystallization process can be detected and the information about their subsequent growth can be obtained. As a result, the (metal-induced) crystallization temperatures reported by in situ TEM/HRTEM are often lower than those determined by other methods and should be regarded as more accurate estimates.

2.3.5 Atomic force microscope (AFM)

Atomic force microscope (AFM) is very useful for surface observation at the nanoscale. AFM is an unparalleled tool for observing temporal changes in the morphology of various materials. It scans the surface of a sample with a sharp tip. The tip is attached to a cantilever, which bends in response to the force applied to it by the sample.

Figure 2.6 shows the schematic of AFM, which consists of two main modules [11]. The first module is the piezoelectric scanner, which moves the sample in the X, Y, and Z axes. The AFM detecting system is the second module. Laser source, cantilever, mirror, photodiode, photodetector, and computer control are all part of this system.

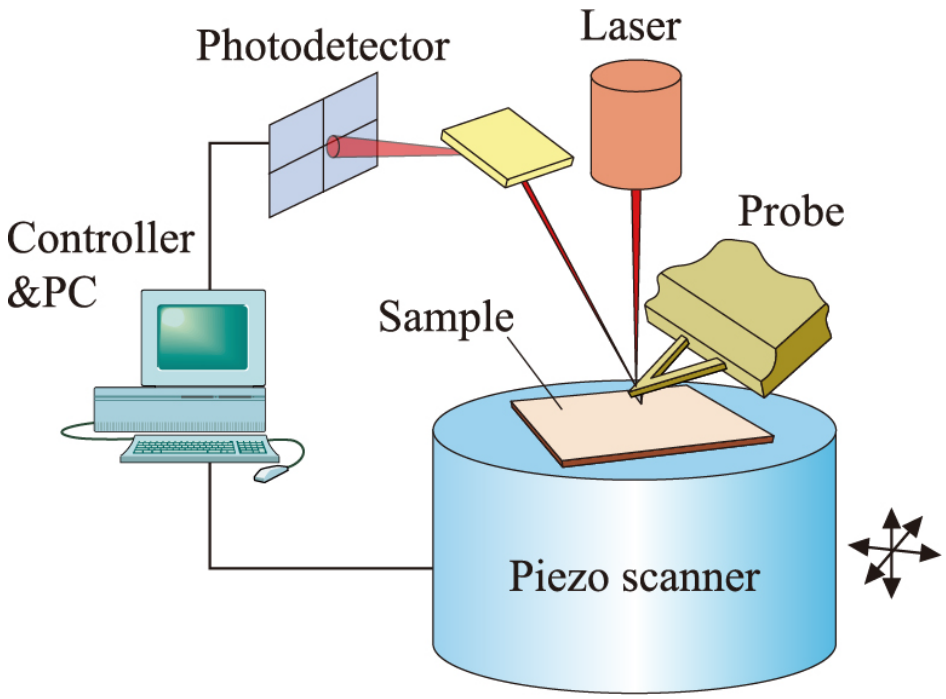

Fig. 2.6. Schematic of an atomic force microscopy setup [11].

The laser is focused onto the back of the reflective cantilever. The laser beam is rebounded off the cantilever and into the photodiode as the tip scans the sample's surface. The photodetector receives the difference in light intensities between the higher and lower photodiodes, and the signal is subsequently delivered to the computer control feedback loop. The feedback loop aims to maintain a constant distance between the cantilever and the sample by keeping the cantilever deflection constant. This can be accomplished by moving the scanner in the Z direction at each (X, Y) location, hence altering the voltage delivered to the scanner. After that, the voltage is transformed into a cantilever deflection. Si_3N_4 or silicon are the most common materials for cantilever tips.

2.4 Experimental methods for investigating the electrical properties

2.4.1 Thin-film transistor (TFT)

Thin-film transistor (TFT) is one of the various applications of Ge thin films including solar cells, thermoelectric generators and rechargeable batteries. TFT is a type of transistor that operates basically on the same principles as MOSFET. It has three terminals: source, drain and gate. The source is typically grounded, the drain collects carriers, and the gate facilitates the establishment of the conductive channel via which the carriers travel from source to drain.

One of the primary distinctions between TFT and MOSFET is that TFT layers may be deposited on a variety of substrates, including flexible substrates. There are four configurations, which may be classified as top gate or bottom gate, as in MOSFETs, and further classified into two groups based on whether the gate is on the same or opposing side of the electrodes (source and drain). These two types are known as coplanar and staggered, respectively [12, 13]. Otherwise, if the source and drain lie between the semiconductor and insulator layers, the structure is considered to be staggered; otherwise, it is a coplanar structure. Figure 2.7 depicts the four TFT structures.[12].

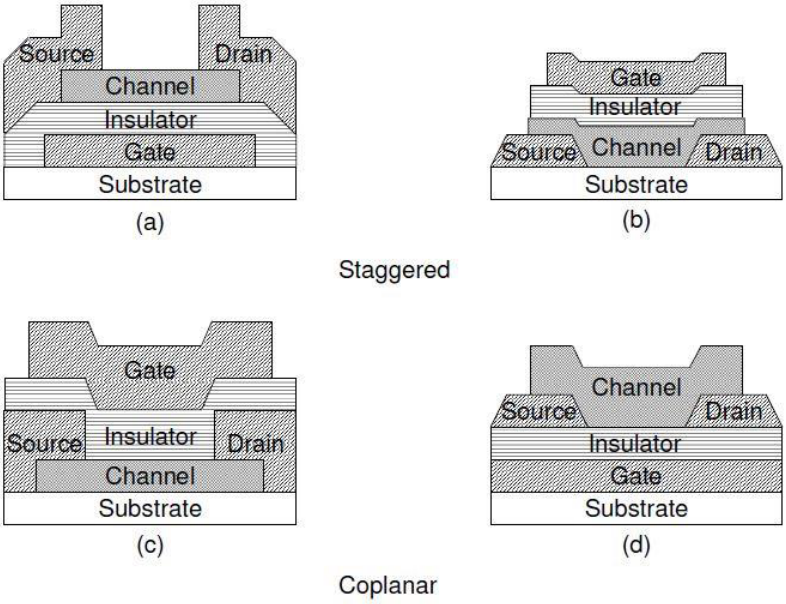

Fig 2.7. Four structures of TFT [12].

The designed structure depends on the application. The staggered configuration is suitable for a-Si TFTs because it minimizes series resistance while ensuring adequate overlap between the electrodes and the active channel layer. Due to the necessity for a high annealing temperature and a flat homogeneous layer, the coplanar structure is appropriate for poly-Si TFT [14].

2.4.2 Hall effect measurement

Hall effect measurement is one of the most powerful methods to analyze the electrical properties of thin film semiconductors, which is extensively used to determine carrier density and mobility. The standard Hall geometry is shown in Fig. 2.8. The Lorentz force, which is a combination of two independent forces: electric and magnetic, is the essential physical principle enabling the Hall effect. When an electron moves along the electric field direction perpendicular to an applied magnetic field, it experiences a magnetic force $-qv \times B$ acting normal to both directions. From Fig. 2.8, a constant current (I) flows along the x-axis direction (left to right) in the existence of a z-directed magnetic field. The Lorentz force causes electrons to drift away from the current direction and toward the negative y-axis, causing an excess negative surface electrical charge on this

side of the sample. This charge results in the Hall voltage, a potential drop across the two sides of the sample [15].

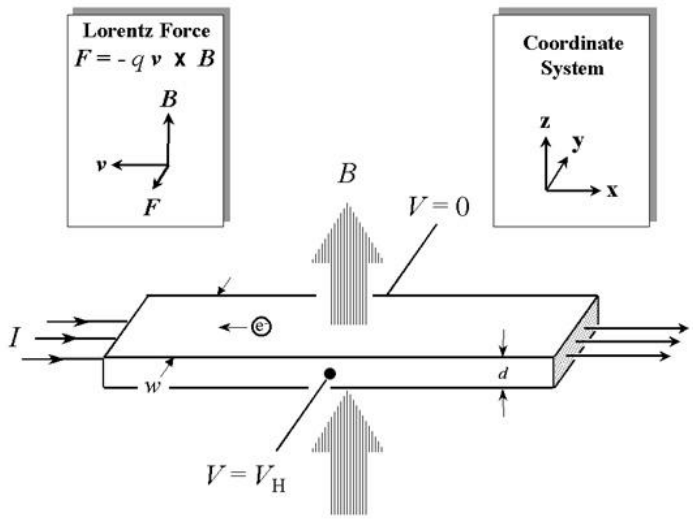

Fig. 2.8. Schematic of the Hall effect in a long thin bar of semiconductor with four ohmic contacts [15].

The combination of resistivity measurement and Hall measurement must be conducted to measure both the carrier mobility and density. The van der Pauw technique is a very useful method due to its convenience and is widely used in the semiconductor industry to investigate the resistivity of uniform samples. As originally devised by van der Pauw, one can use an arbitrarily shaped, thin-plate sample containing four very small ohmic contacts placed on the periphery (preferably in the corners) of the plate. A schematic of a rectangular van der Pauw configuration is shown in Fig. 2.9 [15].

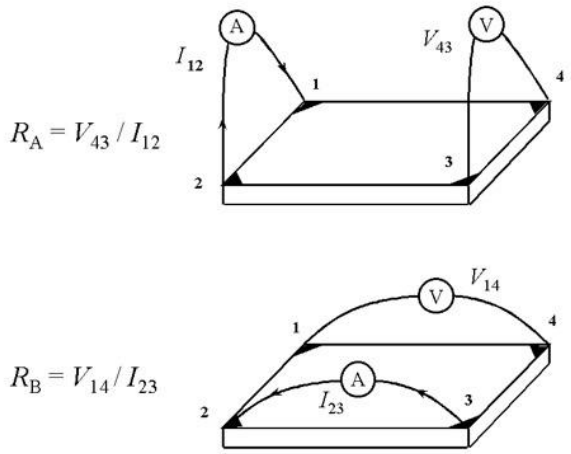

Fig. 2.9. Schematic of a van der Pauw configuration used in the determination of the two characteristic resistances R_A and R_B [15].

The aim of the Hall effect measurement in the van der Pauw technique is to investigate the carrier density by measuring the Hall voltage. The Hall voltage is measured with a constant current and a constant magnetic field applied perpendicular to the sample plane. The identical sample, as illustrated in Fig. 2.10, can be utilized for the resistivity measurement as well. A current is driven across the opposing pair of contacts 1 and 3, and the Hall voltage is measured across the remaining pair of contacts 2 and 4. The carrier density can be calculated once the Hall voltage has been obtained [15].

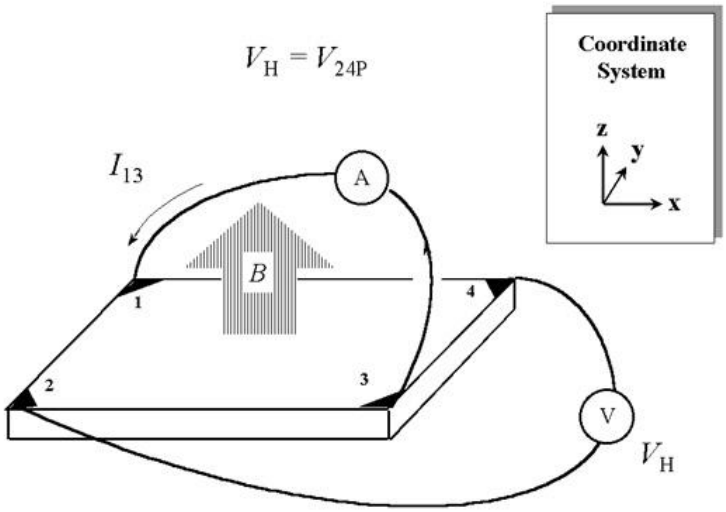

Fig. 2.10. Schematic of a van der Pauw configuration used in the determination of the Hall voltage [15].

In the investigation of Hall and resistivity measurements, there are a few practical considerations to keep in mind. (1) Ohmic contact quality and size, (2) sample homogeneity and precise thickness determination, (3) thermomagnetic effects owing to nonuniform temperature, and (4) photoconductive and photovoltaic effects, which can be mitigated by measuring in a dark environment, are the primary considerations. In addition, the sample lateral dimensions must be large in comparison to the contact size and sample thickness. Finally, sample temperature, magnetic field strength, electrical current, and voltage must all be correctly measured [15].

It is better to fabricate the samples from thin semiconductor plates with the appropriate geometry, as shown in Fig. 2.11. The average diameters of the contacts, and sample thickness must be much smaller than the distance between the contacts [15].

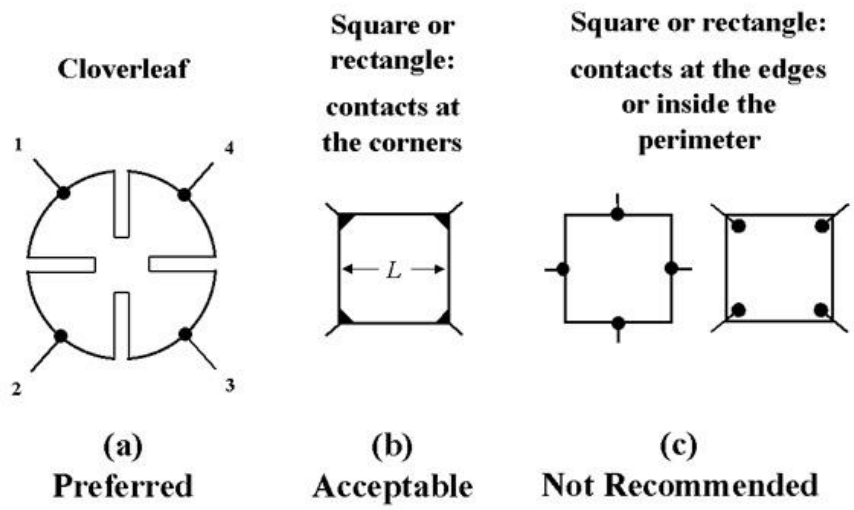

Fig. 2.11. Sample geometries for van der Pauw resistivity and Hall effect measurements [15].

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Chapter 3

Effect of initial Au and Ge layer thicknesses on the crystallization process of Ge thin films

3.1 Introduction

In this chapter, the details of the effect of Au and Ge layer thickness on the crystallization process of Ge thin films by Au-induced layer exchange at low temperature without the introduction of interfacial insert layer are described. The influence of Au layer thickness on Ge crystallization behavior is studied. It has been found that Ge crystals are (111) oriented when the Au layer is as thin as 9 nm, whereas crystal grains are randomly oriented when the Au layer is as thick as 34 nm. The influence of Ge layer thickness on Ge crystallization behavior was also studied. It is found that the formation of a double crystalline Ge layer structure is observed with the bottom layer having a higher crystal quality. An almost uniform Ge crystalline layer is obtained by adjusting the initial Ge thicknesses and a Hall effect hole mobility of ~85 cm^2/Vs is achieved for a film as thin as 30 nm. These findings will open up the possibility to apply the MIC technique to crystallize Ge thin films at temperatures as low as ~220°C, which is low enough to fabricate thin-film semiconductor on various inexpensive plastic substrates.

3.2 Experimental methods

3.2.1 Sample preparation

In this work, Au film was used as a catalyst to crystallize Ge thin films. Si wafers with 100 nm thick thermally grown oxides were used as substrates. These substrates were cleaned by acetone and ethanol using an ultrasonic cleaning bath for 10 min each prior to the sputtering process. Au (target: 99.99%, deposition rate: 0.72 nm/s) and amorphous Ge (a-Ge) (target: 99.999%, deposition rate: 0.32 nm/s) layers are successively deposited on these substrates by RF magnetron sputtering process with Ar plasma (Ar gas purity 99.9999%, pressure during deposition: 3×10^{-3} Torr) to form an a-Ge/Au bilayer.

3.2.2 Effect of initial Au layer thickness

To look at the effect of initial Au layer thickness on the crystallization process, the Au layer thickness is varied from 9 to 34 nm, while the a-Ge layer thickness is kept constant at 30 nm. The process is schematically shown in Fig. 3.1(a). The crystallization process was observed by in-situ x-ray diffraction (XRD) experiment in the θ-2θ mode with a scattering vector normal to the film surface using a built-in heating chamber under N_2 ambient with temperatures ranging from 100°C to 300°C. The heating profile is schematically shown in Fig 3.1(b).

The crystallization process has also been investigated by ex-situ Raman measurements and scanning electron microscope (SEM) observation. Isochronal (10 min) cumulative annealing from 100 to 220°C with a 10°C increment under N_2 ambient has been performed. The heating profile is schematically shown in Fig 3.1(c). After each heat treatment, the sample was cooled down to room temperature to perform Raman measurements and SEM observation. After annealing at 220°C, electron backscatter diffraction (EBSD) measurement has been performed to identify the crystal orientation after selectively etching Au with KI and I_2 solution. To examine the electrical properties of the Ge thin films, TFTs were fabricated using these films as channel layers. After selectively etching Au, the Au film (~40 nm) was deposited onto Ge film as source and drain electrodes through a metal mask by thermal evaporation technique. The highly doped Si substrates with thermally grown oxide layers have been used as gate electrodes.

Additionally, Hall effect measurement has also been employed to evaluate the electrical properties of these Ge thin films.

3.2.3 Effect of initial Ge layer thickness

To determine the effect of initial a-Ge layer thickness on the crystallization behavior by Au-induced layer exchange, Au (fixed at 29 nm) films were deposited on a Si substrate and subsequently a-Ge (ranging from 27-55 nm) films were fabricated on top of the Au layers. The films were crystallized by MIC technique at 220°C for 1hr with a 10°C/min heating rate under N_2 ambient and cooled down naturally to room temperature. The sample structure and crystallization process are schematically shown in Fig. 3.2. The crystallization behavior was observed by x-ray diffraction (XRD) in the θ-2θ mode with a scattering vector normal to the film surface. The cross-section of the film was observed by transmission electron microscopy (TEM).

After selectively removing Au by a solution containing KI and I_2, the quality of Ge crystal was investigated by Raman spectroscopy with a 532-nm laser excitation. The surface morphology was observed by both scanning electron microscope (SEM) and atomic force microscopy (AFM). Electron backscatter diffraction (EBSD) measurement has been performed to identify the crystal orientation. To examine the electrical properties of the Ge thin films, TFTs were also fabricated with the same condition as the experiment to investigate the effect of initial Au layer thickness. Additionally, Hall effect measurement has also been employed to evaluate the electrical properties of Ge thin films.

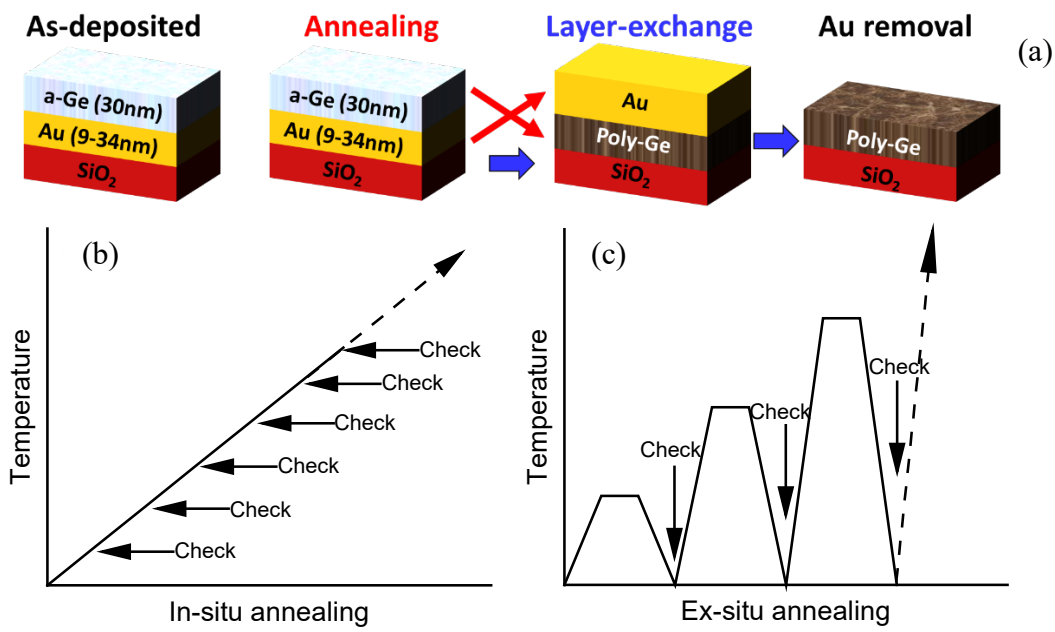


Fig. 3.1. Effect of initial Au layer thickness: (a) The process is schematically shown. The schematics of the heating profile in (b) in-situ XRD and (c) ex-situ Raman measurement and SEM observation.

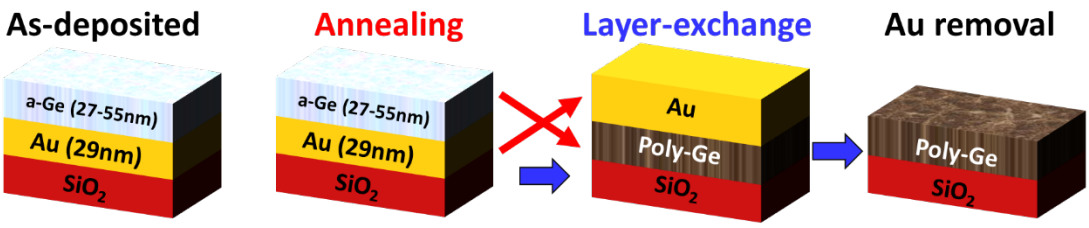


Fig. 3.2. Effect of initial Ge layer thickness: schematic of Ge film on SiO_2 substrate.

3.3 Results and discussion

3.3.1 Effect of initial Au layer thickness on Ge film properties

3.3.1.1 Chemical composition of Ge films by EDS analysis

The EDS measurement was used to clarify the existence of layer exchange phenomena for this experiment. Typical EDS spectra of the as-deposited and annealed (200°C) samples with initial Au layer thickness of 34 nm, which are measured by using the low-energy electron beam with an acceleration voltage of 3 keV, are shown in Fig. 3.3. A low-energy electron beam has been employed to make the measurement surface sensitive. For the as-deposited sample, the Ge peak at ~1.2 keV is much larger than the Au peak at ~2.1 keV, because 30 nm of Ge layer exists on top of the Au layer. However, the clear Au peak appeared for the sample annealed at 200°C for 10 min, which implies the existence of a layer exchange between the Ge and Au layers [1-3]. The difference in the color of the sample surface is also confirmed in the sample photographs (inset of Fig. 3.3).

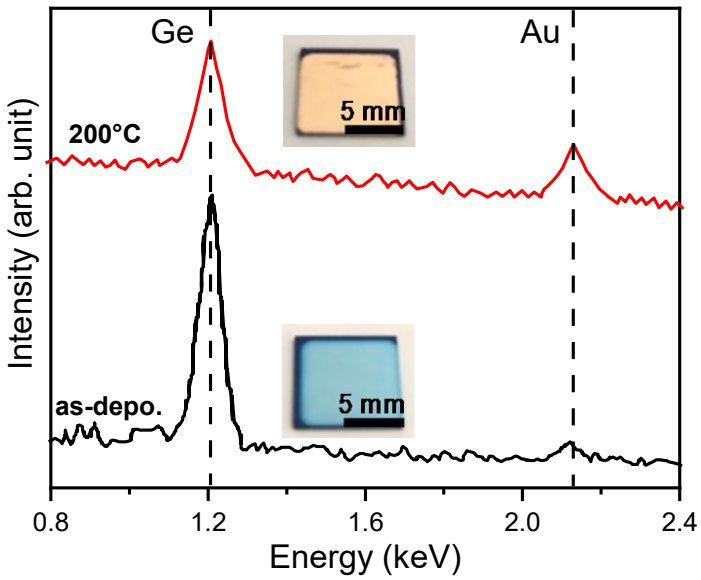


Fig. 3.3. Typical EDS spectra and photographs of Au(34nm) sample in the as-deposited state and after heat treatment at 200°C.

3.3.1.2 Evaluation of crystallinity of Ge films by in-situ XRD observation

The crystallinity for Ge thin films was evaluated by XRD measurement with the θ-2θ configuration. Figure 3.4 shows the XRD profiles of the samples after annealing at 220°C. The diffraction from the Ge (111) plane is clearly observed around 27.3º, which suggests that the Ge layer is crystallized during the annealing process at this temperature. The (111) diffraction is the only appreciable peak for Ge. The intensity of the Ge (111) diffraction shows the largest value for the Au(9nm) sample and decreases as the Au layer thickness increases. Additionally, it is seen that the Au layers are (111) oriented.

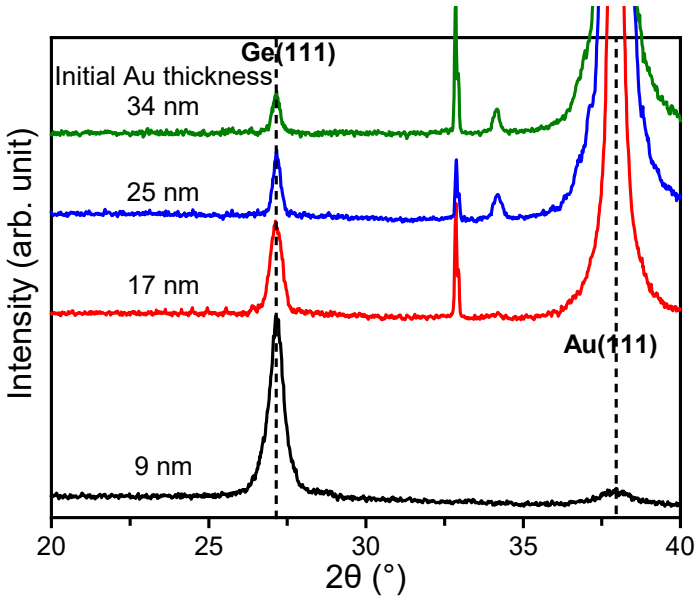


Fig 3.4. In-situ XRD profiles of all samples at 220°C. The sharp peak at 33° is the forbidden Si (200) diffraction from the substrate.

The evolution of the Ge (111) intensity obtained from this in-situ experiment from 100°C to 300°C is plotted in Fig. 3.5. The Ge (111) diffraction peaks start to appear at a temperature as low as 140°C. This is in accordance with the TEM observations where Ge crystal nucleation promoted by Au takes place at a temperature lower than 150°C [4, 5]. The peak seems to appear at a lower temperature for samples with thinner Au films. The intensity increases rapidly up to ~200°C and increases gradually afterwards.

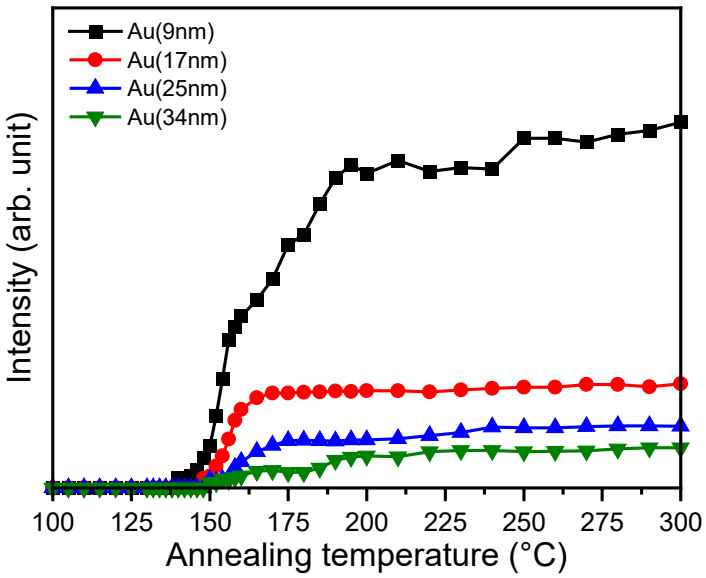


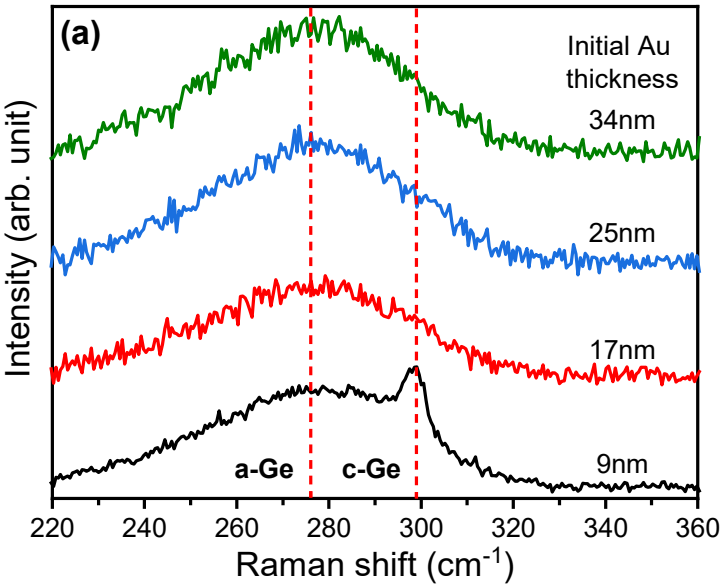
Fig 3.5. Evolution of the Ge (111) diffraction intensity during in-situ XRD measurement.

3.3.1.3 Film structure investigation by ex-situ Raman measurement

The film structure was also characterized by ex-situ Raman spectroscopy during isochronal (10 min) cumulative annealing from 100°C to 220°C. Figure 3.6(a) shows the Raman spectra of all samples after annealing at 110°C. Although a broad peak around 275 cm^{-1}, which corresponds to a-Ge, is the main feature, a sharp peak due to the Ge-Ge vibration mode in c-Ge around 300 cm^{-1} is identified for the Au(9nm) sample. This implies that the nucleation of Ge crystals already starts at a temperature as low as 110°C for this sample and implies a higher nucleation rate for the thinner Au sample. The existence of the Ge crystal grain was indeed confirmed by SEM, which is shown in Fig. 3.6(b). The amount of crystal at this low temperature might not have been large enough to be detected by XRD. The fact that crystallization is confirmed only for Ge(30nm)/Au(9nm) at this temperature implies either the effect of Au layer thickness and/or substrate surface on crystallization.

Raman spectra after isochronal cumulative annealing at 220°C are shown in Fig. 3.7(a). The main feature is the sharp peak around 300 cm^{-1}, which suggests that the Ge crystallization has already taken place at this annealing temperature. Raman shift and full width at half maximum (FWHM) of the Ge films as a function of temperature are shown in Figs. 3.7(b) and (c), respectively. The increase in Raman shift and decrease of FWHM up to ~180°C corresponds to the growth of Ge crystalline grains which is in accordance

with the evolution of Ge (111) XRD intensity in Fig. 3.5 [6, 7]. As the Au layer thickness decreases, the Raman shift decreases and the FWHM of the peaks increases. This implies that the Ge crystalline grains are smaller for Ge films crystallized by a thinner Au catalyst.



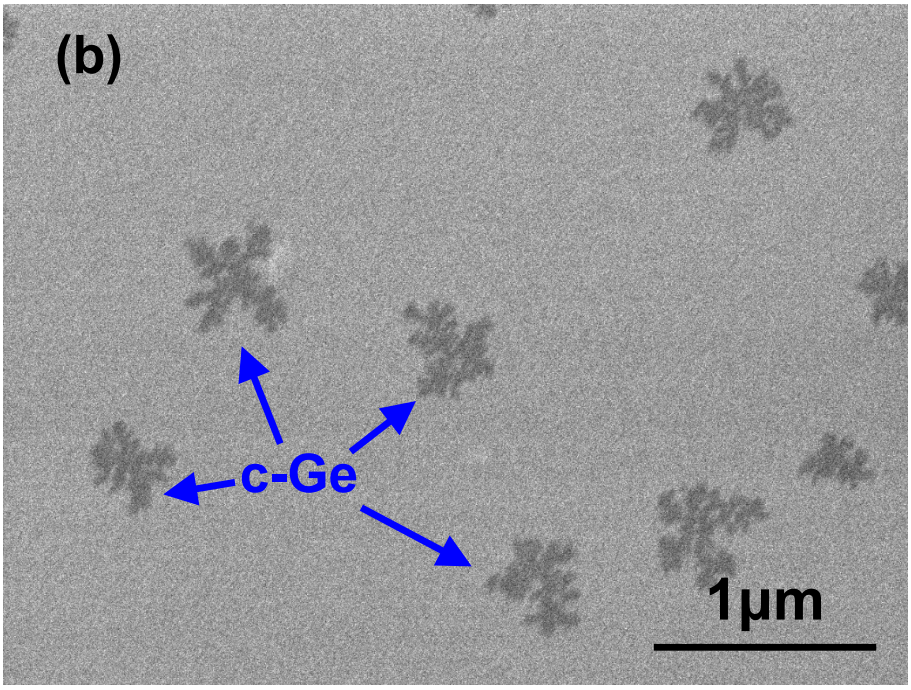


Fig. 3.6. (a) Raman profiles of all samples annealed at 110°C. (b) SEM image of Au(9nm) sample annealed at 110°C.

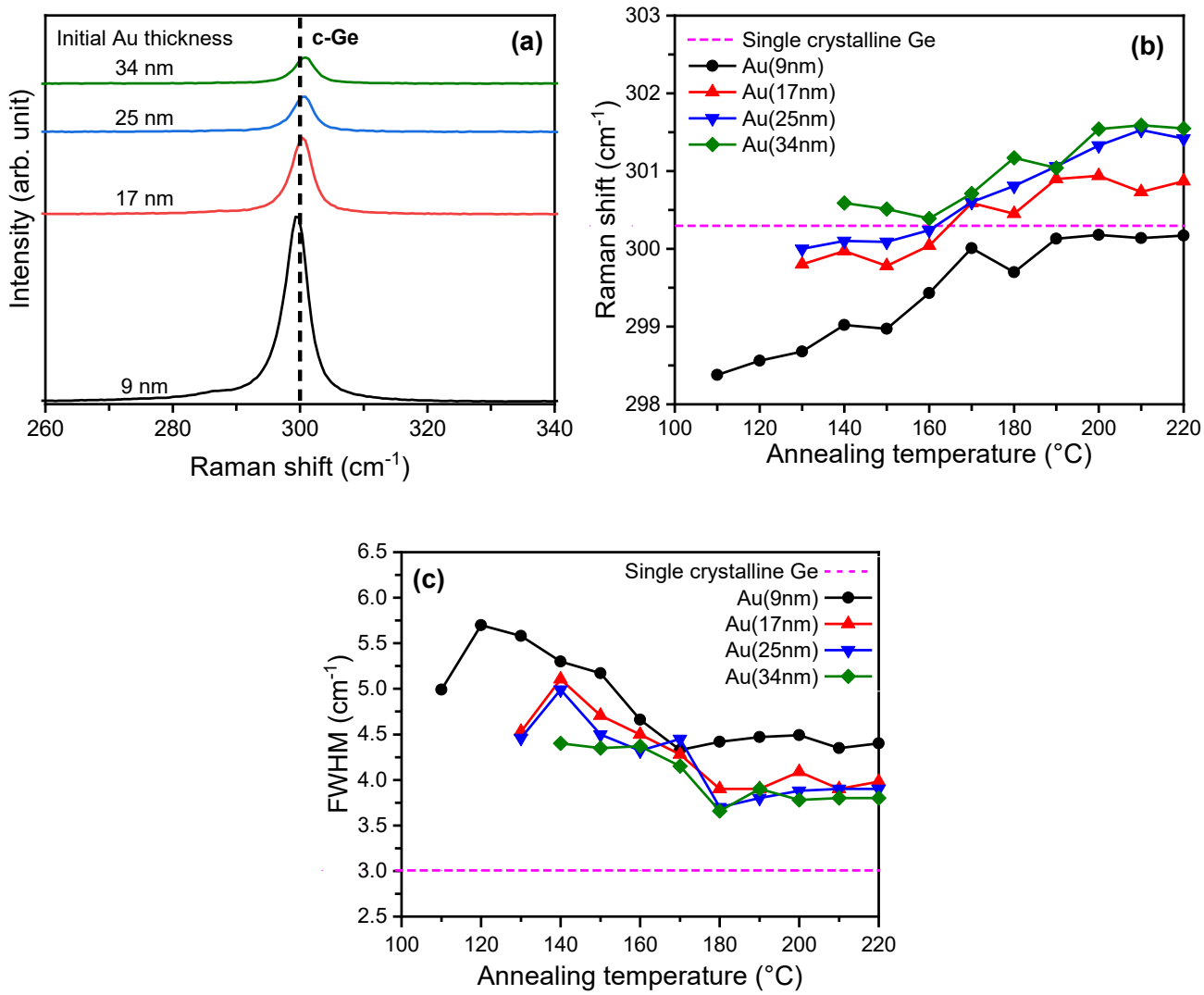


Fig. 3.7. (a) Raman spectra of all samples annealed at 220°C. (b) Evolution of the Raman shift of crystalline Ge of all samples. (c) Evolution of the FWHM values of the Raman peak of crystalline Ge of all samples.

3.3.1.4 Growth evolution of crystalline Ge examined by SEM observation

Figure 3.8 shows the SEM micrographs of the samples after annealing at 150°C and 220°C. Ge crystals, which correspond to black dots in the images, are already visible at 150°C. The density of Ge crystal grains after heat treatment at 150°C obtained from these SEM images are summarized in Fig. 3.9. The density is larger for thinner Au layer samples, which implies a higher nucleation rate.

As the annealing temperature increases, Ge diffuses into the Au layer. Since AuGe is a eutectic system, phase separation into crystalline Ge and FCC Au occurs at some Ge concentration, as directly observed by TEM experiments [8]. Since Ge diffusion is blocked at the Au/SiO_2 interface in our study, the increase of Ge concentration in Au is more rapid for thinner Au layers. Moreover, the SiO_2 surface could promote nucleation of Ge crystals. These factors could lead to higher nucleation rates for samples with thinner Au layers. The evolution of the grain density and percentage of total coverage of crystalline Ge for the initial Au(34nm) sample obtained from the SEM images are shown in Fig. 3.10. It is seen that the number of grains is already saturated at 150°C and further crystallization proceeds by the growth of each grain by the addition of Ge atoms from the amorphous phase. As will be discussed in the next chapter, Ge atoms are supplied through Au to the c-Ge nucleus to promote further growth.

In the TEM study [9], it was found that an Au grain boundary acts as a nucleation site and nucleation has been observed at a temperature as low as 130°C. The fact that the grain density is already saturated at 150°C in the present study suggests that the nucleation of c-Ge at the Au grain boundary has already completed at this temperature and growth takes place at a higher temperature.

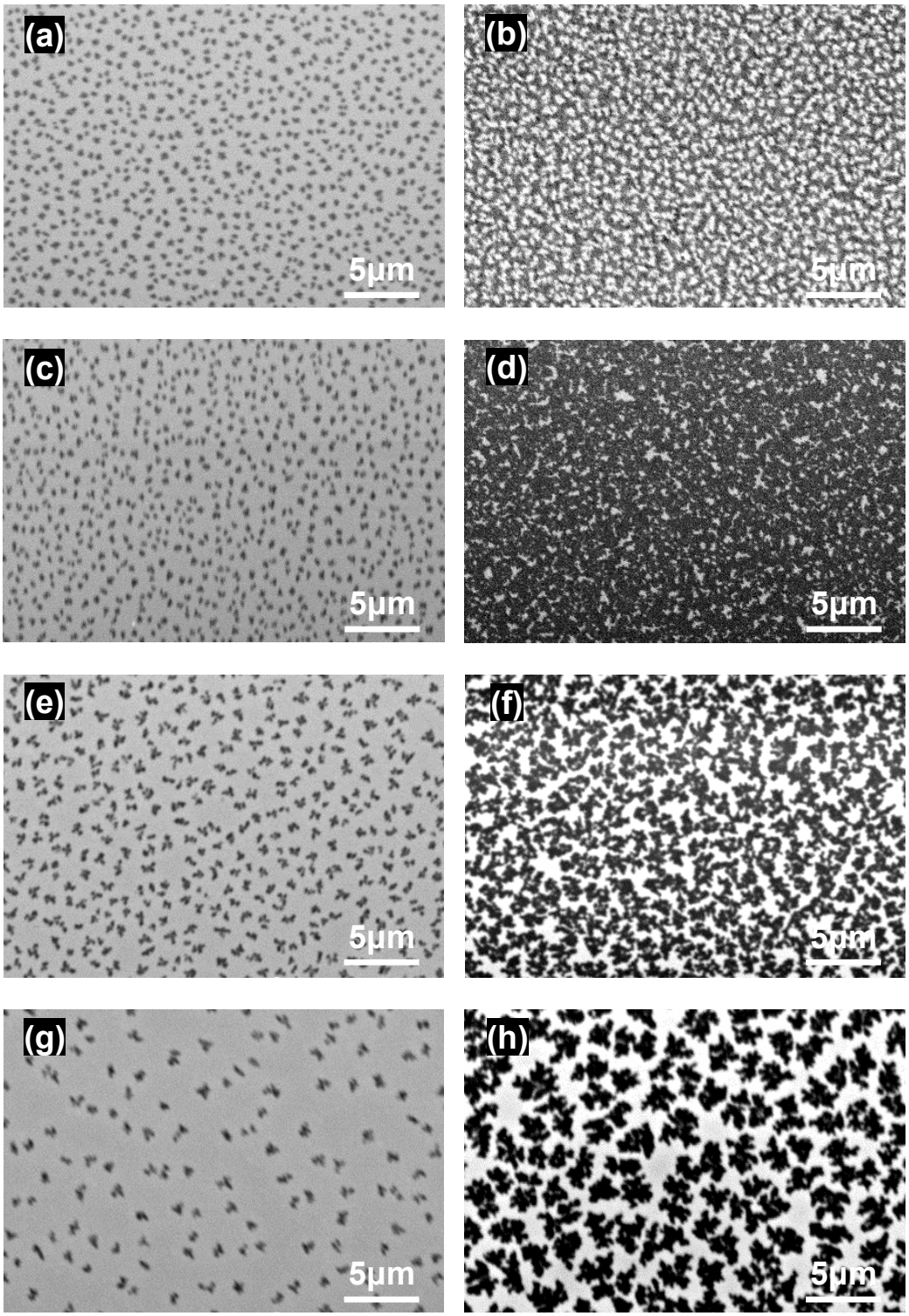


Fig. 3.8. SEM images of Au(9nm) annealed at (a) 150°C and (b) 220°C; Au(17nm) annealed at (c) 150°C and (d) 220°C; Au(25nm) annealed at (e) 150°C and (f) 220°C; Au(34nm) annealed at (g) 150°C and (h) 220°C.

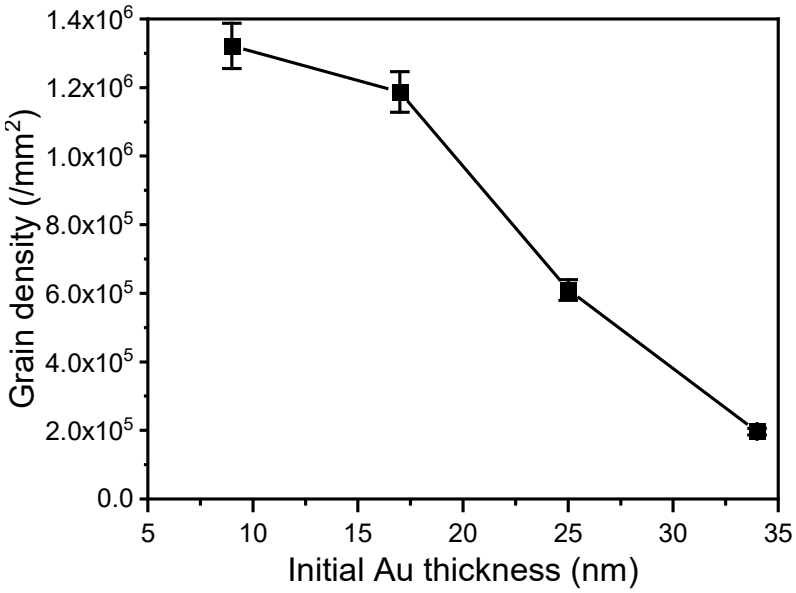


Fig. 3.9. Density of Ge crystal grains after annealing at 150°C.

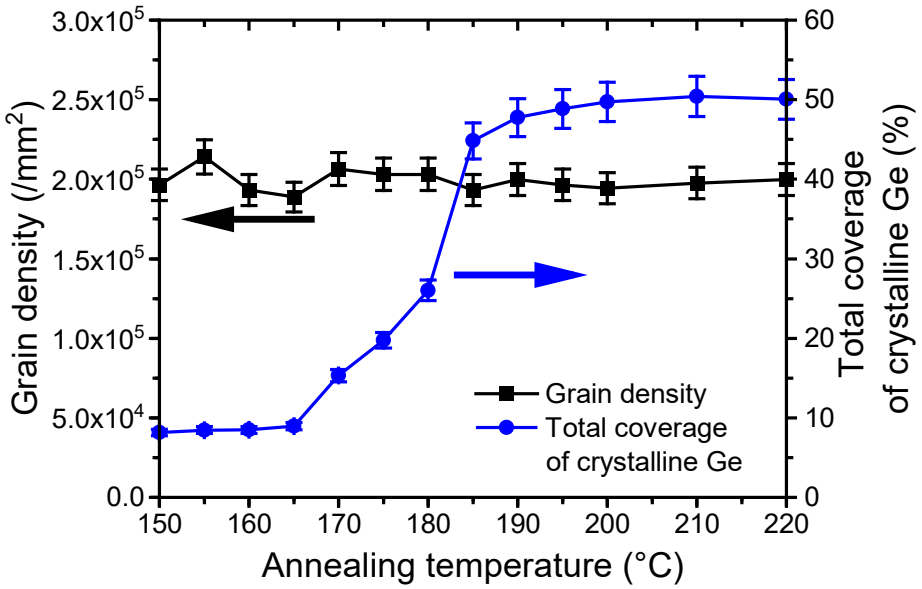


Fig. 3.10. Evolution of the grain density and total coverage of crystalline Ge for the Au(34nm) sample as a function of annealing temperature.

3.3.1.5 Observation of surface morphology by SEM observation

To clarify the details of surface morphology of Ge films after crystallization by ex-situ annealing, images by FE-SEM have also been obtained. Figure 3.11 shows the SEM images of the samples annealed at 220°C. Au on the surface was selectively etched by KI and I_2 solution before observation. The bright area corresponds to crystalline Ge and this area seems to decrease as the Au layer thickness increases. Although the resolution is not enough in Fig. 3.11(a), clear evidence of Ge island growth on the Ge layer (second layer) is not identified in Figs. 3.11(b), (c) and (d) as has been observed in the Al/Ge system [10, 11]. This implies that the Ge concentration in the Au layer is not high enough to form a second layer for thicker Au samples.

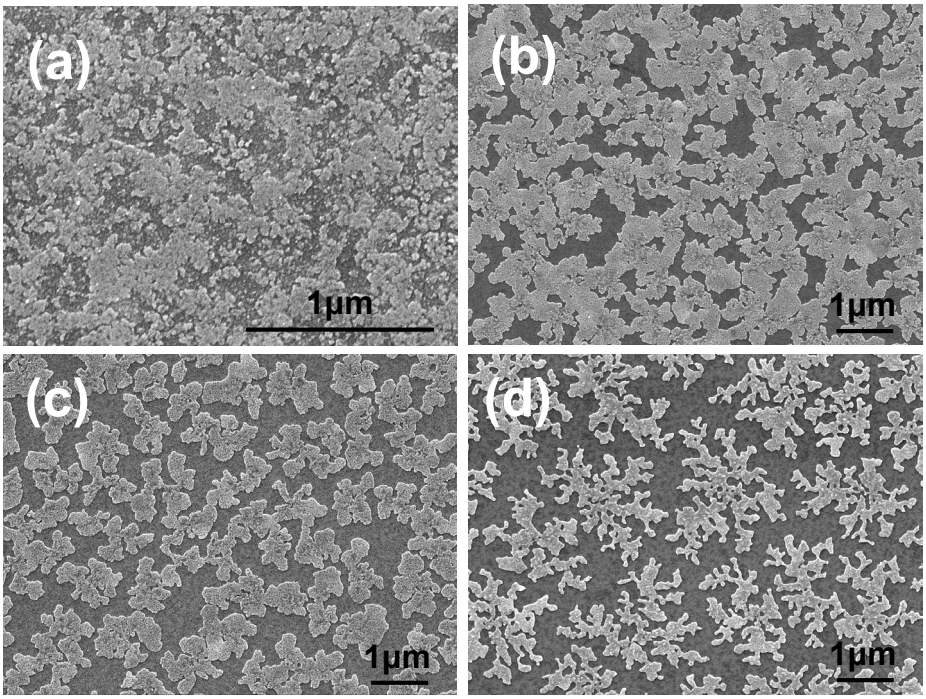


Fig. 3.11. SEM images of (a) Au(9nm), (b) Au(17nm), (c) Au(25nm) and (d) Au(34nm) samples annealed at 220°C.

3.3.1.6 Examination of crystal orientation by EBSD measurement

EBSD measurements were also performed for these Ge thin films to evaluate crystal orientation. Figure 3.12 shows the EBSD images which show the Ge crystal orientation normal to the film plane. The corresponding SEM images of the same area are also shown. The image of the Au(9nm) sample, Fig. 3.12(a), shows that the film is mainly (111) oriented, which is in accordance with a large intensity of the Ge (111) diffraction in the XRD profile in Fig. 3.4. The size of each crystal grain is smaller than 1μm, which agrees with the Raman measurement results. As the Au layer thickness increases, the fraction of (111) orientation decreases, which is also in accordance with the XRD profiles. Each dendritic grain visible in the SEM image in Fig. 3.12(d) is composed of several crystal grains.

These results suggest that the Au thickness has a profound effect on the crystal orientation of the crystallized Ge thin film. Considering Ge diffusion into the Au layer during the annealing process, Ge concentration should be larger near the a-Ge/Au interface in the Au layer than near the Au/SiO_2 interface. Therefore, nucleation of crystalline Ge is likely to occur near the a-Ge/Au interface. The crystal orientation is random for samples with thicker Au layers in the present study, which implies that the anisotropy in the interface energy between Au and c-Ge is small [12]. On the other hand, the crystalline Ge film crystallized in the Ge(30nm)/Au(9nm) sample is exclusively (111) oriented. When the Au layer is as thin as 9nm, the nucleation site should be close also to the Au/SiO_2 interface and SiO_2 surface is likely to promote Ge crystal to orient in the (111) direction to minimize the interfacial energy between crystalline Ge and the SiO_2 surface. Toko et al. have investigated the effect of substrates on the Ge crystal orientation and found that an amorphous substrate tends to orient the Ge crystal in the (111) orientation, which is in accordance with the present result [13, 14]. The SiO_2 surface could have also promoted the heterogeneous nucleation of crystals, which led to lower crystallization temperature and smaller grain sizes for thinner Au samples.

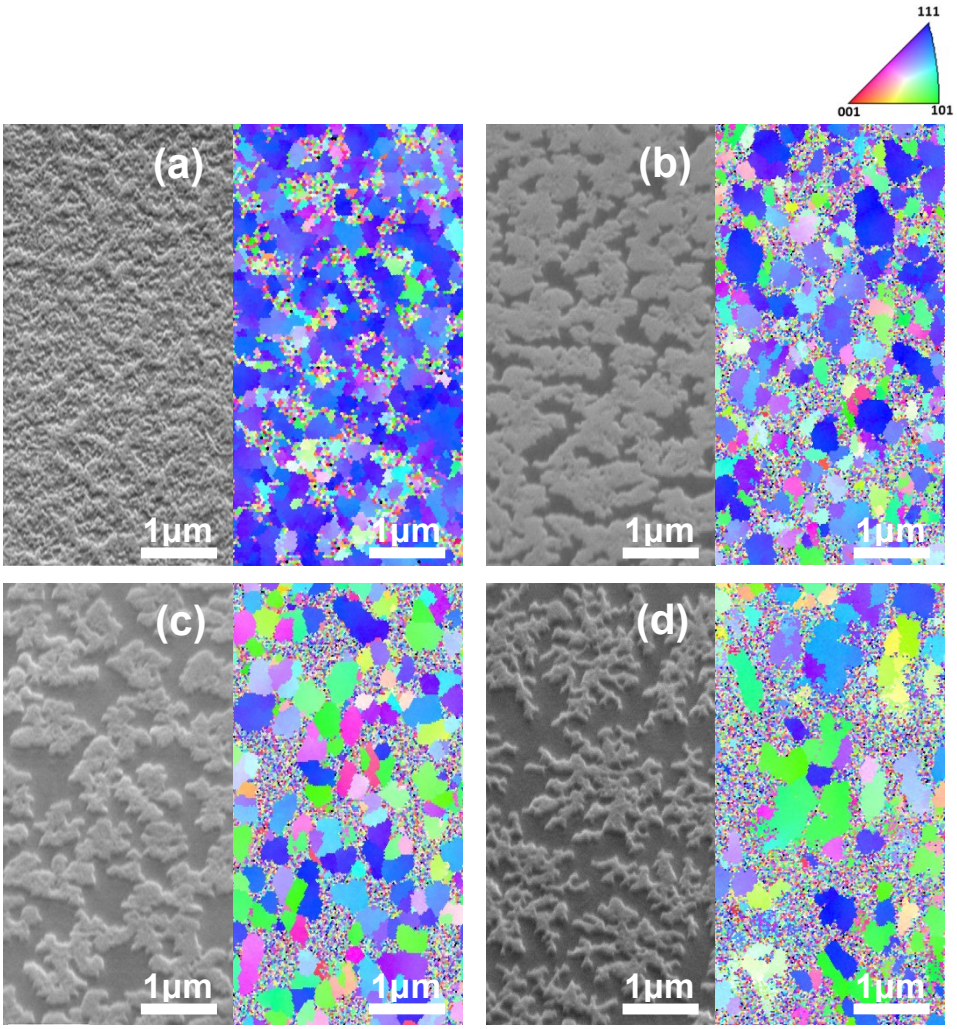


Fig. 3.12. EBSD images of Ge crystal orientation normal to the film plane of (a) Au(9nm), (b) Au(17nm), (c) Au(25nm) and (d) Au(34nm) samples annealed at 220°C

3.3.1.7 Electrical property evaluation by Hall effect measurement and TFT operation

The electrical properties have also been characterized by Hall effect and TFT measurements for the Au(9nm) sample. Figure 3.13 shows the output characteristic I_{ds}/V_{ds} and transfer characteristic I_{ds}/V_{gs} curves of the TFT fabricated from the Ge layer crystallized by annealing the Au(9nm) sample. The TFT action is successfully demonstrated. Moreover, Hall effect mobility of as high as ~50 cm^2/Vs is achieved for this sample. However, other films did not show the TFT action probably because the films were not continuous.

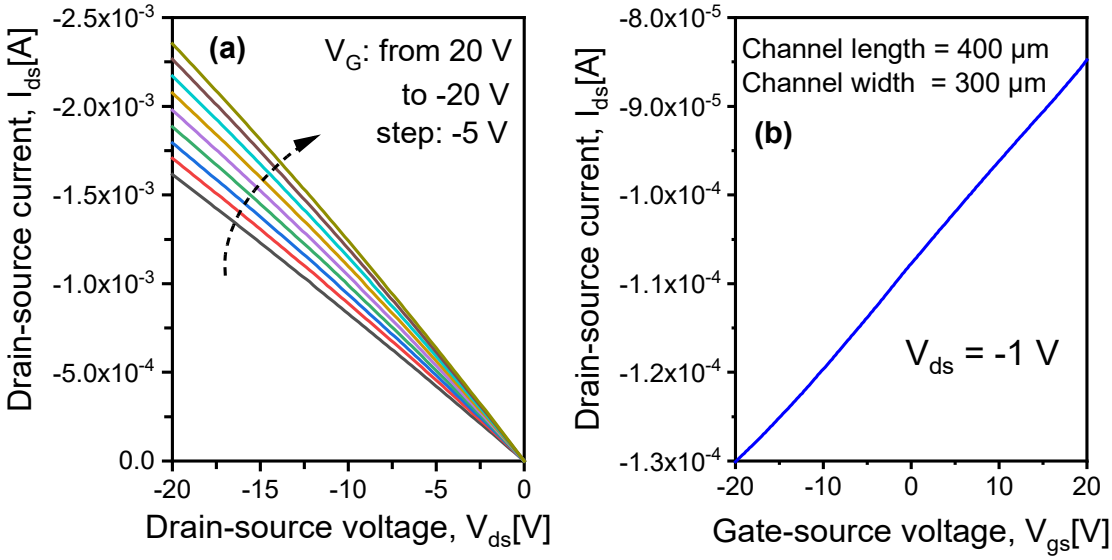


Fig. 3.13. (a) Output characteristics I_{ds}/V_{ds} and (b) transfer characteristics I_{ds}/V_{gs} of the TFT fabricated by using a Ge thin film obtained by annealing a Au(9nm) sample at 220°C.

3.3.2 Effect of initial Ge layer thickness on Ge film properties

3.3.2.1 Crystallization characteristics by XRD observation

The crystallization of Ge films has been investigated by XRD measurement. Figure 3.14 shows the XRD profiles of Ge films crystallized by the MIC technique using Au as catalyst. The Au thickness in this experiment was fixed at 29 nm. The Ge thin films were annealed at 220°C for 1 hr before structural investigation. The Ge (111) diffraction peaks around 27.3º are clearly observed, which shows that Ge is crystallized at this temperature. However, the peak intensity does not drastically change as a function of Ge thickness, which implies that the initial Ge thickness does not have so much effect on the crystal orientation.

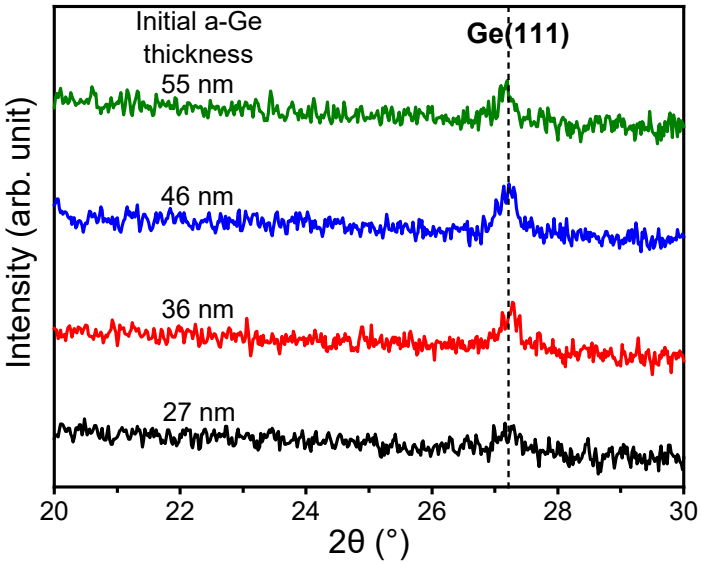


Fig. 3.14. XRD profiles of Ge films obtained after annealing at 220°C for 1 hr.

3.3.2.2 Crystal quality investigation by Raman measurement

The Raman measurement was also performed in order to evaluate the crystal quality of Ge films after Au layer was removed by KI and I_2 solution. Figure 3.15 shows the Raman spectra of Ge films grown by annealing at 220°C. Clear sharp peaks appear around 300 cm^{-1} which indicates that a-Ge films were successfully crystallized by MIC at 220°C, which is in accordance with the XRD results.

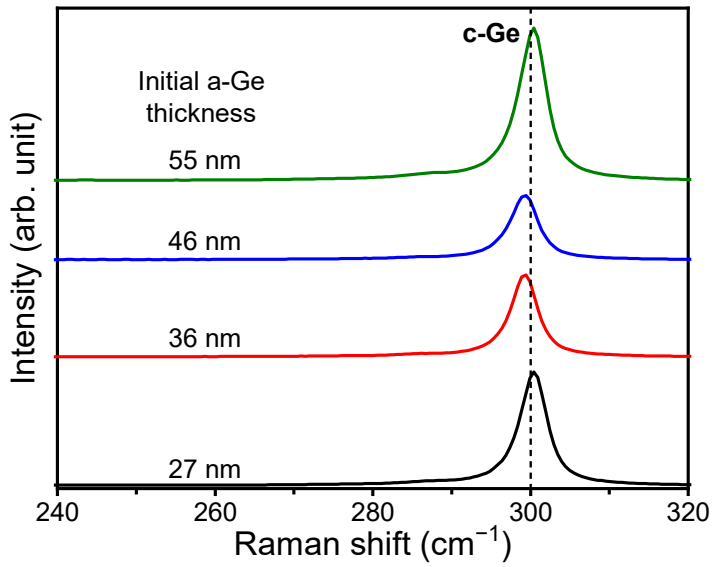


Fig. 3.15. Raman spectra of Ge films obtained after annealing at 220°C for 1 hr.

To estimate the crystal quality of the Ge films, Raman shift and full width at half maximum (FWHM) of the Ge films as a function of initial Ge thickness are given in Fig. 3.16. The Raman shift and FWHM of single crystalline Ge are also indicated for comparison. The peak position (Raman shift) of Ge(27nm) is close to that of the single crystal. However, the peak position decreases as the initial Ge thickness increases and increases again as the initial Ge thickness reaches 55 nm. On the other hand, the FWHM of Ge films slightly increases as a function of initial Ge thickness.

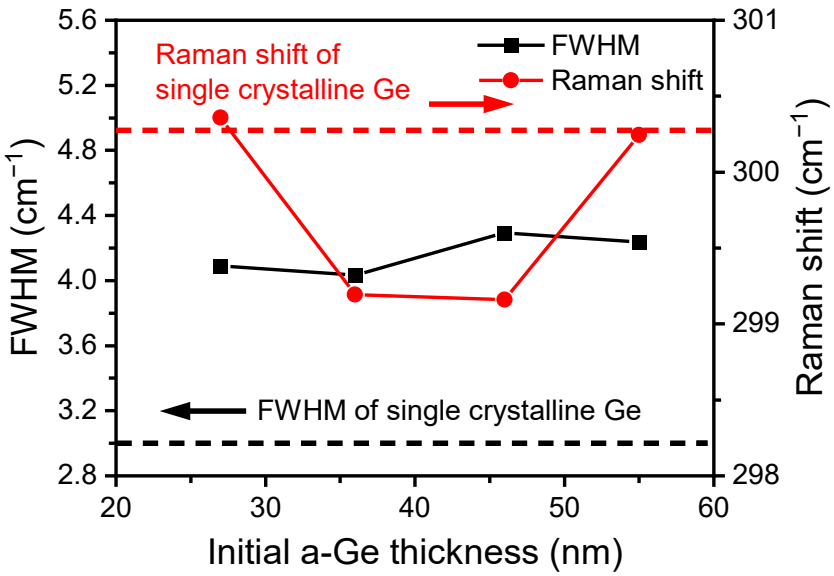


Fig. 3.16. Raman shift and FWHM of Ge films obtained after annealing at 220°C for 1 hr.

3.3.2.3 Surface morphology observation by SEM and AFM observation

Figure 3.17 shows the SEM micrographs of the samples after annealing at 220°C for 1 hr. Au was selectively removed by the wet etching process in KI and I_2 solution before observation. Crystalline Ge are clearly observed for all samples. In Figs. 3.17(a) and (b), crystalline Ge layers and bare SiO_2 surfaces are clearly observed. The uncovered SiO_2 area decreases as the initial Ge thickness increases up to 46 nm. ~97 % of the surface is covered with crystalline Ge when the initial Ge layer thickness is 46 nm as can be seen in Fig. 3.17(c). However, a small protrusion (white dot) is observed and this feature increases as the Ge layer thickness is increased up to 55 nm, Fig. 3.17(d). This protrusion seems to be a second layer formed on the first layer.

The same kind of surface morphology is confirmed in the AFM images for these samples as in Fig. 3.18. The white areas in SEM image turn out to be the second layer of Ge formed on the first layer. The three surfaces of SiO_2, bottom Ge layer and top Ge layer, are clearly observed in Fig. 3.17(d) which is in accordance with the AFM image in Fig. 3.18(d). The same kind of morphology is observed for Ge films crystallized by Al-induced crystallization [10, 11].

The coverage of the first and second layers of c-Ge obtained from the SEM images in Fig. 3.17 was analyzed by the ImageJ program and is plotted in Fig. 3.19 as a function of the initial a-Ge layer thickness. The coverage of the first layer increases up to an a-Ge layer thickness of 46 nm, where ~97% of the substrate surface is covered by c-Ge.

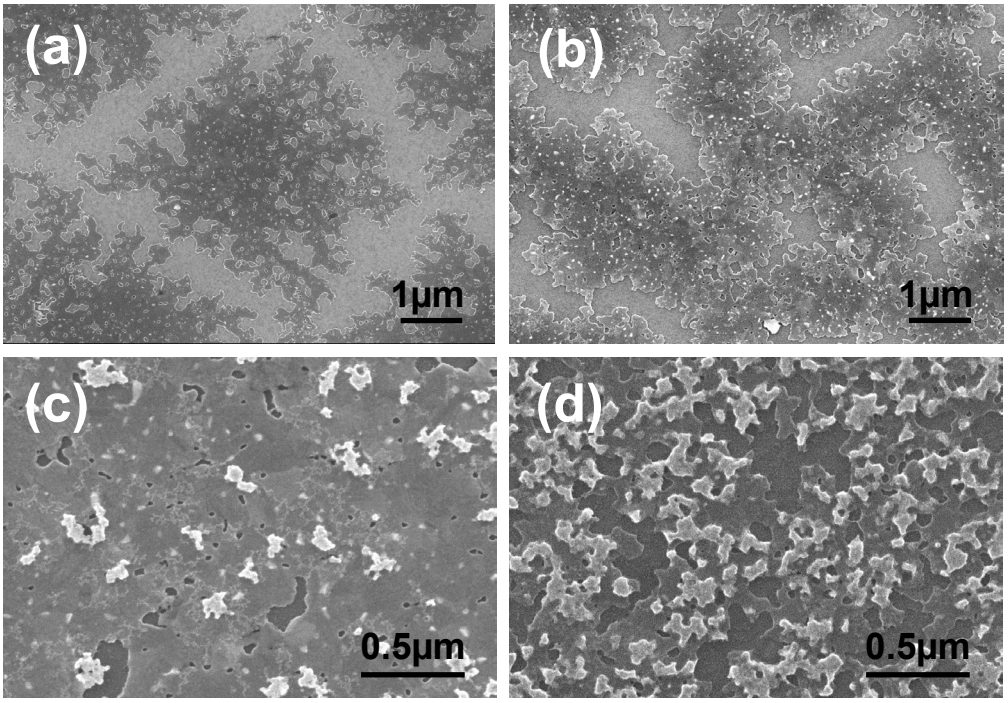


Fig. 3.17. SEM images of Ge films obtained after annealing the following samples at 220°C for 1 hr. (a) a-Ge(27nm), (b) a-Ge(36nm), (c) a-Ge(46nm) and (d) a-Ge(55nm).

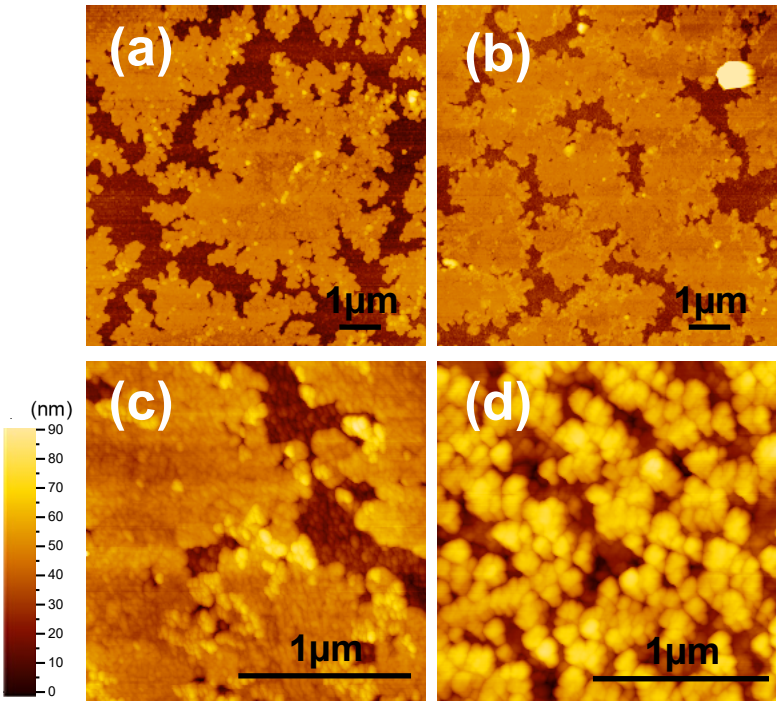


Fig. 3.18. AFM images of Ge films obtained after annealing the following samples at 220°C for 1 hr. (a) a-Ge(27nm), (b) a-Ge(36nm), (c) a-Ge(46nm) and (d) a-Ge(55nm).

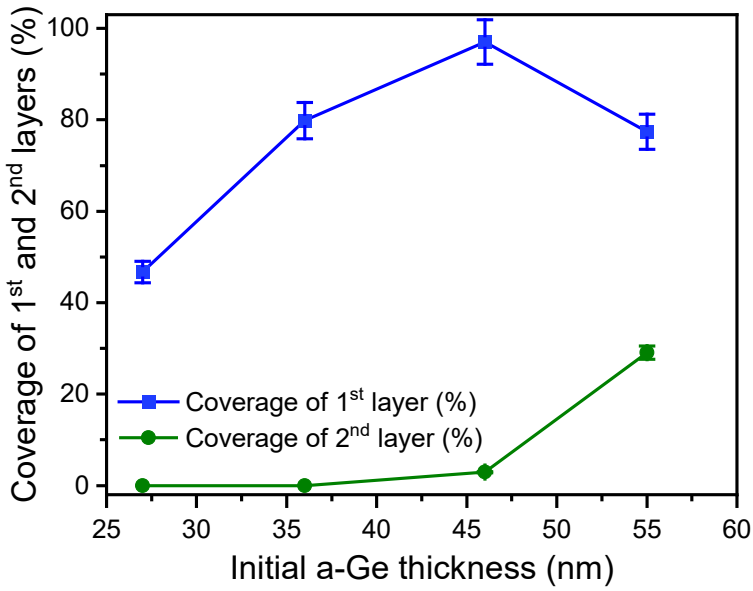


Fig. 3.19. Coverage of the 1st and 2nd layers of c-Ge as a function of the initial a-Ge thickness.

3.3.2.4 Cross-sectional Ge film structure by TEM observation

The double layer structure was also confirmed in the cross-sectional TEM micrograph of the Ge(55nm) sample after annealing at 220°C for 1 hr as shown in Fig. 3.20. The image was taken without Au removal. A high crystal quality of the first Ge layer is confirmed in the magnified image, Fig. 3.20(b). Moreover, it is seen that the thickness of the first Ge layer is ~30 nm which is close to the original Au layer thickness. This suggests that crystalline Ge has nucleated in the Au layer and grew laterally, as has been observed also for Al/Ge system [11, 12]. In addition to the increase in the amount of second layer for the Ge(55nm)/Au(29nm) sample, Fig. 3.17(d), the increase of uncovered SiO_2 is confirmed. This morphology could have affected the strain in the film and contributed to the sudden increase of the Raman shift as in Fig. 3.16.

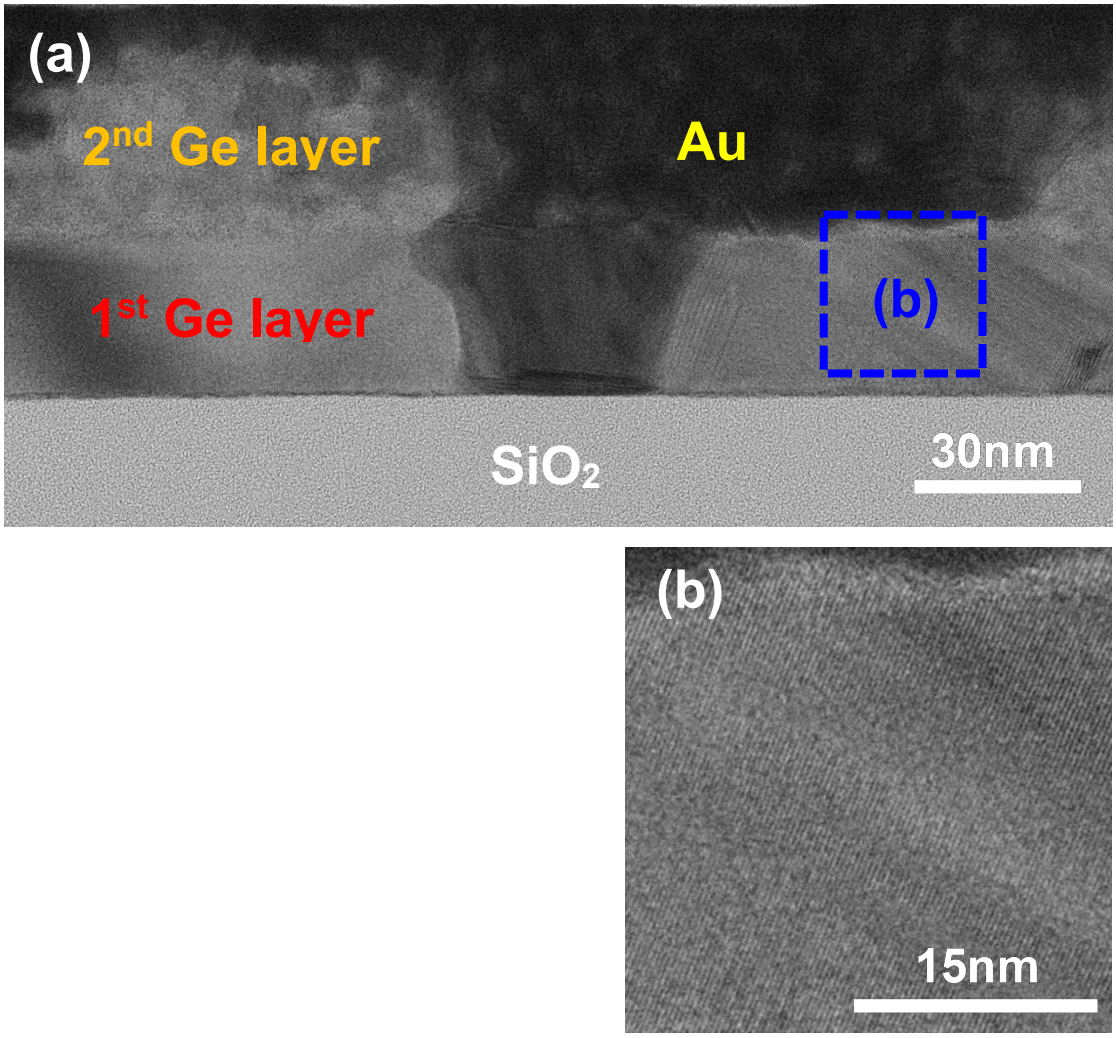


Fig. 3.20. Cross-sectional TEM image of a-Ge(55nm) sample after annealing at 220°C for 1 hr. (a) Low magnification and (b) high magnification bright-field images.

These results suggest that the crystallization mechanism of the Au/Ge system resembles that of Al/Si and Al/Ge systems [11, 12, 15, 16]. First, Ge atoms diffuse into the Au layer to form an alloy. At some Ge concentration, c-Ge will nucleate by phase separation because Au/Ge is a eutectic system. The nucleated c-Ge will grow laterally, which will account for the same thicknesses of the original Au layer and the resulting first layer of c-Ge. As c-Ge occupies the bottom region, Au will move upwards to complete layer exchange. It seems that the second layer is composed of small grains, which implies a different crystallization mechanism. The Au diffused into the a-Ge layer might have contributed to the crystallization of Ge without layer exchange.

3.3.2.5 Crystal orientation investigation by EBSD measurement

EBSD experiment has also been performed to clarify crystal orientation. Figure 3.21 shows the EBSD mapping of Ge films obtained after annealing at 220°C for 1 hr, which shows the Ge crystal orientation normal to the film plane. The corresponding SEM images are also shown. For the a-Ge(27nm)/Au(29nm) sample, Fig. 3.21(a), it is seen that the isolated islands which is clearly observed in the SEM image is composed of many small crystalline grains of few hundred nm, which does not depend so much on the original a-Ge layer thickness. The fact that crystals are not oriented in a specific orientation suggests that the nucleation of crystalline Ge has not occurred on the SiO_2 surface, but near the Au/Ge interface [14]. This implies a higher Ge concentration near the Au/Ge interface due to the diffusion of Ge atoms into the Au layer. Moreover, the fact that each dendritic island consists of small crystallites implies a high nucleation rate of c-Ge. The size of these crystalline grains does not depend so much on the Ge layer thickness, which is in accordance with the almost constant FWHM of Ge Raman peaks in Fig. 3.16. Continuous film with a small number of uncrystallized area is obtained for the Ge(46nm) sample as shown in Fig. 3.21(c). For the Ge(55nm) sample, however, the uncrystallized area increases which is in accordance with SEM and AFM images.

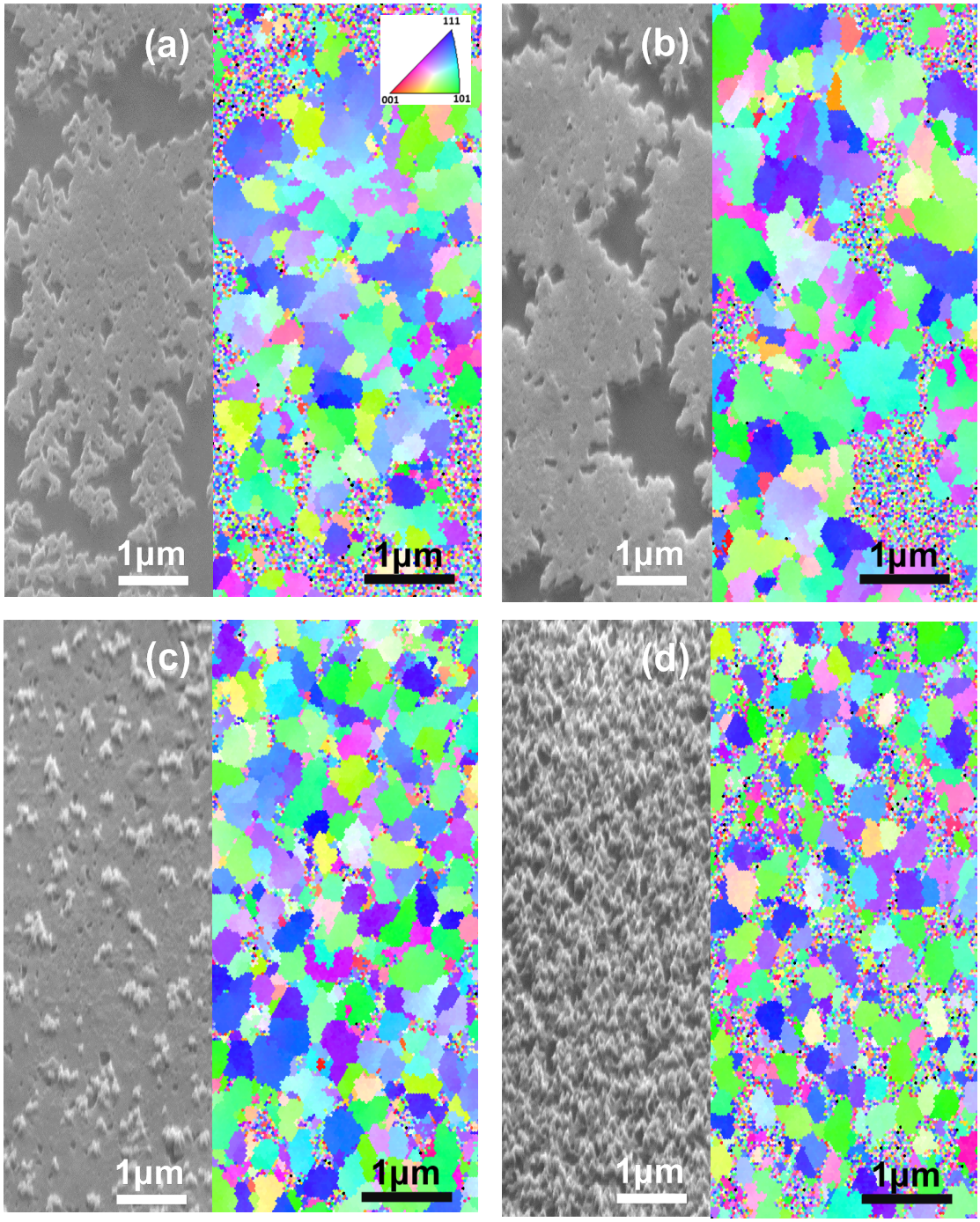


Fig. 3.21. EBSD and SEM images of Ge films obtained after annealing the following samples at 220°C for 1 hr. (a) a-Ge(27nm), (b) a-Ge(36nm), (c) a-Ge(46nm) and (d) a-Ge(55nm). The EBSD images show crystal orientation normal to the film plane.

3.3.2.6 Electrical properties evaluation by Hall effect measurement and TFT operation

To clarify the electrical properties of Ge films crystallized by Au-induced crystallization, the Hall effect measurement has been employed in this experiment. Figure 3.22 shows the carrier mobility of Ge films as a function of initial Ge thickness. A p-type behavior was confirmed for all Ge samples. The highest carrier mobility is achieved for the Ge(46nm) sample which is as high as ~85 cm^2/Vs due to the highest coverage of crystalline Ge, ~97%. The mobility decreases for the Ge(55nm) sample, probably because of the larger area of second layers and voids in the first layer. The measurement could not be performed for the Ge(27nm) sample, however, because the film was not continuous.

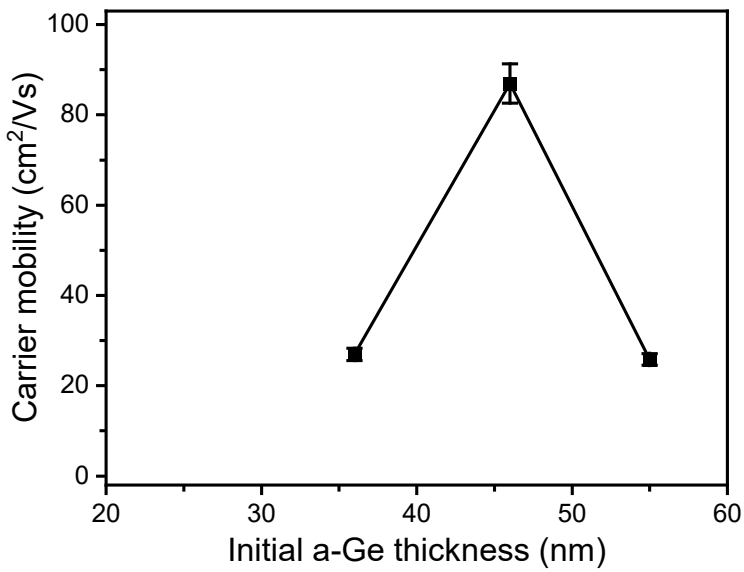


Fig. 3.22. Carrier mobility of Ge films crystallized at 220°C as a function of initial a-Ge thickness.

Although Au acts as an amphoteric impurity in Ge (three acceptor levels and one donor level) [17, 18], the solubility of Au in Ge is negligible (~4×10^9 cm^{-3} at 250°C) [19], and it is likely that holes in Ge have been generated by acceptor levels introduced by vacancies and dangling bonds around grain boundaries and Ge/SiO_2 interface [20-24].

The electrical properties are also evaluated by fabrication of TFTs by using these Ge films as channel layers. Figure 3.23 shows the output characteristic I_{ds}/V_{ds} and transfer characteristic I_{ds}/V_{gs} curves of the TFT fabricated from the Ge layer crystallized by annealing the Ge(46nm) sample. Reflecting the almost complete Ge first layer, a p-type

transistor action is successfully demonstrated, although the on/off ratio is poor, which is a general trend for Ge films crystallized by Au-induced layer exchange [25].

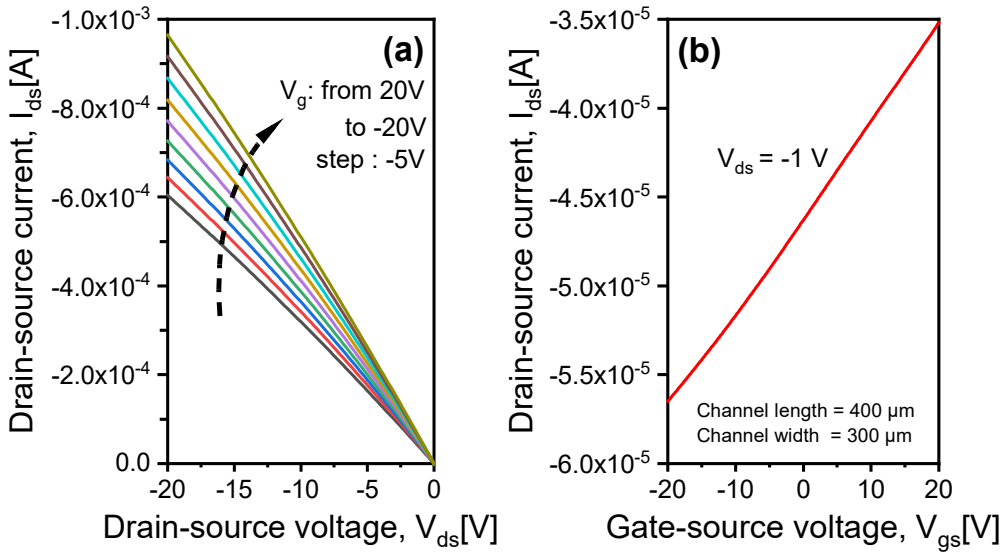


Fig. 3.23. (a) Output characteristics I_{ds}/V_{ds} and (b) transfer characteristics I_{ds}/V_{gs} of the TFT fabricated by using a crystalline Ge thin film obtained by annealing a Ge(46nm) sample at 220°C for 1 hr.

3.4 Conclusion

In this experiment, the Au and Ge layer thickness dependence of the crystallization process by Au-induced crystallization has been investigated. It has been found that the layer exchange occurs even without the insert layer. The effect of initial Au thickness on the crystallization of Ge thin films was first investigated in this experiment. Reducing the Au layer thickness has the effect of inducing Ge (111) orientation and reducing the crystallization temperature. This behavior seems to be brought about by the substrate, and the nucleation position of crystalline Ge seems to be playing an important role in the crystallization process. The SiO_2 surface could have promoted the heterogeneous nucleation of crystalline Ge, which led to lower crystallization temperature, smaller grain sizes and higher (111) orientation. These findings are encouraging in terms of the smaller consumption of rare metals like Au.

Additionally, the effect of initial a-Ge layer thickness on the crystallization of Ge thin films has been investigated. Double layer structure of crystalline Ge has been found with the bottom layer having a higher crystal quality and the thickness close to the original Au layer. This morphology resembles that of crystalline semiconductor thin films obtained by annealing Al/Si and Al/Ge systems. It is possible to control the coverage of the bottom c-Ge layer by adjusting the initial a-Ge thickness, and nearly 97% of the substrate surface is covered by the bottom c-Ge layer by annealing an a-Ge(46nm)/Au(29nm) bilayer at 220°C. The resulting ~30nm thick Ge film shows a hole mobility of as high as ~85 cm^2/Vs reflecting a high coverage. These findings will open up the possibility to apply the MIC technique to crystallize Ge thin films at temperatures as low as ~220°C, which is low enough to fabricate thin-film semiconductor on various inexpensive plastic substrates. A further improvement in mobility is expected by increasing the size of each Ge crystallites constituting a dendritic c-Ge grain.

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Chapter 4

Crystallization mechanism of Ge thin films by Au-induced layer exchange

4.1 Introduction

In chapter 3, it is found that the layer exchange type crystallization occurs even in the absence of the insert layer. In this chapter is described the details in Ge crystallization behavior during the Au-induced layer exchange process, and the crystallization mechanism is discussed. The results show that the nucleation of c-Ge occurs mainly inside the bottom Au layer. The c-Ge grows laterally, and the Au is pushed-up to complete layer exchange. It is also found that the excess Ge forms the second c-Ge layer on the first layer and the growth of the second layer occurs at a higher temperature compared to the first layer. This behavior can be used to suppress the growth of the second layer and decrease the surface roughness, which will be discussed in detail in the next chapter.

4.2 Experimental methods

In this experiment, Au film was used as a catalyst for Ge film crystallization. Si wafers with 100 nm thick thermally grown oxides were used as substrates. These substrates were cleaned by acetone and ethanol using an ultrasonic cleaning bath prior to the sputtering process. Au (target: 99.99%, deposition rate: 0.72 nm/s) and a-Ge (target: 99.999%, deposition rate: 0.32 nm/s) layers are successively deposited on these substrates by RF magnetron sputtering process with Ar plasma (Ar gas purity 99.9999%, pressure during deposition: 3×10^{-3} Torr) to form an a-Ge/Au bilayer. The Au and a-Ge layer thickness are fixed at 29 and 46 nm, respectively. The schematic structure of Ge film on SiO_2 substrate for this experiment is shown in Fig. 4.1(a). To look at the growth evolution of crystalline Ge, the in-situ x-ray diffraction (XRD) experiment was performed in the θ-2θ mode with a scattering vector normal to the film surface using a built-in heating chamber under N_2 ambient with temperatures ranging from 100 to 300°C. The temperature profile is schematically shown in Fig 4.1(b). The growth evolution of crystalline Ge was also observed by ex-situ scanning electron microscope (SEM) and cross-sectional transmission electron microscopy (TEM). The maximum annealing temperature for each segment is increased by 10°C from 120 to 220°C. The heating rate was 10°C/min under N_2 ambient. The temperature profile is schematically shown in Fig 4.1(c).

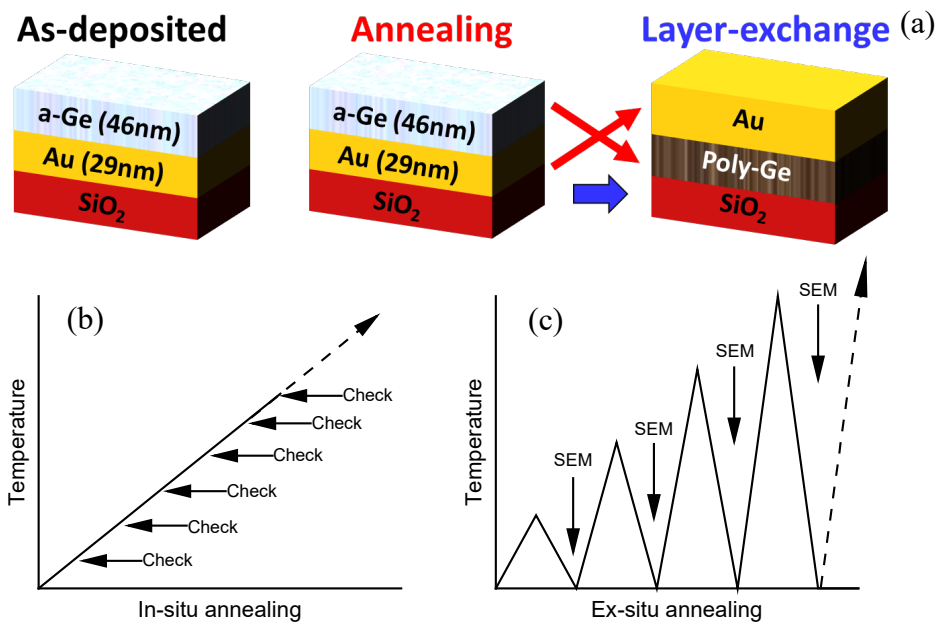

Fig. 4.1. (a) Schematic structure of Ge film on SiO_2 substrate. Heating profiles for (b) in-situ XRD experiment and (c) ex-situ SEM and TEM observation.

4.3 Results and discussion

4.3.1 Investigation of the formation of crystalline Ge films

The evolution of the Ge (111) and Au (111) diffraction intensity obtained from the in-situ XRD experiment from 100 to 300°C is plotted in Fig. 4.2. The Ge (111) diffraction peak start to appear at a temperature around 160°C which is a bit higher than in the previous chapter. This is due to differences in the initial Au and Ge thicknesses. The Ge (111) intensity rapidly increases up to ~180°C. It is seen that the Au (111) intensity increases up to ~150°C and then suddenly decreases up to ~180°C.

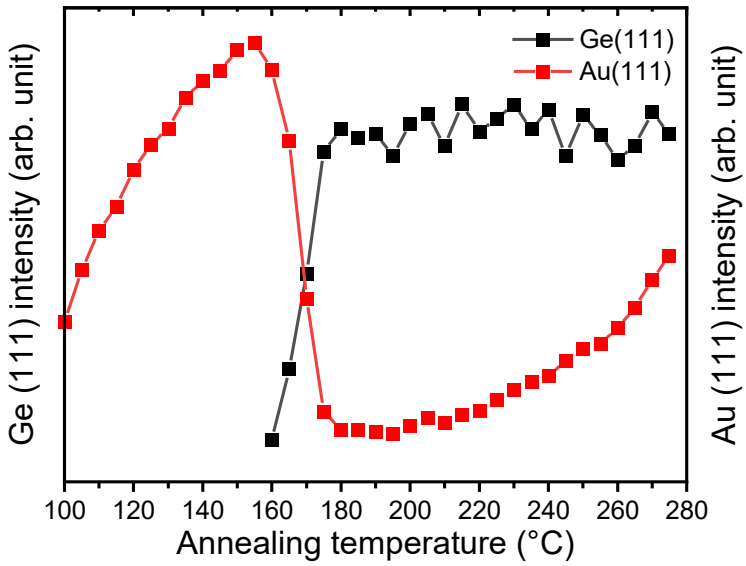

Fig. 4.2. Evolution of the Ge (111) and Au (111) diffraction intensity during in-situ XRD measurement.

Figure 4.3 shows the SEM images during the decrease of Au (111) XRD intensity during the annealing process. It is seen that the reacted area increases as the Au(111) intensity decreases and almost all the area has reacted at 175°C. The decrease in the Au (111) XRD intensity could be attributed to the layer exchange process.

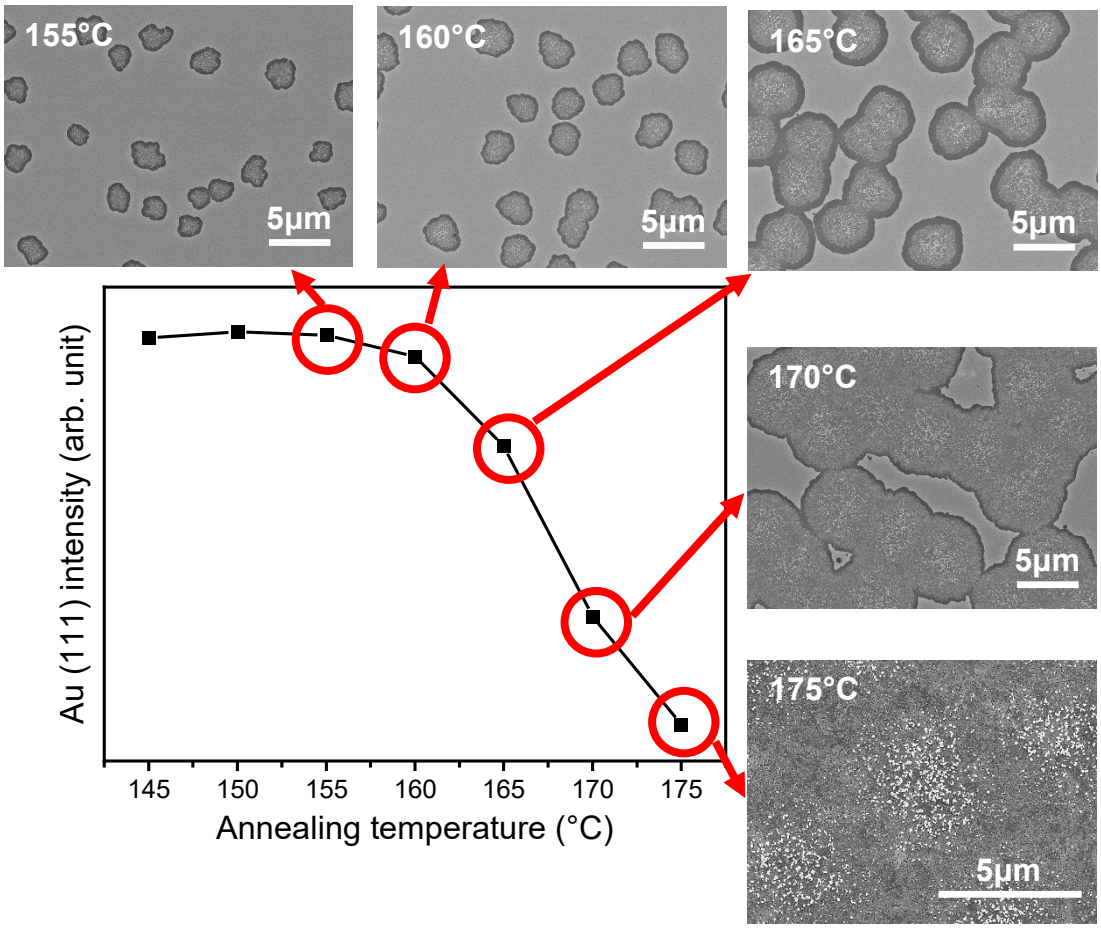

Fig. 4.3. The SEM images of the Au(29nm)/Ge(46nm) sample during the decrease of the Au(111) XRD intensity.

To look at the growth evolution in detail, the SEM and TEM observation have been performed. The annealed Au(29nm)/Ge(46nm) sample was observed by SEM and TEM after each annealing segment which is schematically shown in Fig 4.1(c). The nucleation of Ge film depends on the Au/Ge layer thickness. In the previous chapter (chapter 3), we found that the nucleation of Ge thin film started at 110°C for the Au(9nm)/Ge(30nm) sample, for which sample the nucleation starts at the lowest temperature because of the thin Au layer. Therefore, in this experiment, the starting temperature is set at 120°C.

At the annealing temperature of 120 and 130°C, the surface is very smooth, and we could not detect any reacted region. Figure 4.4 shows the SEM image of the Ge film after annealing at 140°C. The small dendritic black dots were detected, which are likely to be crystalline Ge nucleated after annealing at 140°C. The amount of crystal is so small

that the existence of the crystal was not observed in the in-situ XRD experiment (Fig. 4.2). Before c-Ge nucleation, Ge atoms from the a-Ge layer diffuse into the Au layer during annealing to form an alloy. When the Ge concentration in Au is supersaturated, c-Ge will nucleate by phase separation because Au/Ge is a eutectic system. This is schematically shown in Fig. 4.4(b). The existence of c-Ge confirmed by cross-sectional TEM is also shown in Fig. 4.5. The image was taken without Au removal. It is seen that the c-Ge nucleated only inside the Au layer and has the same thickness as the Au layer.

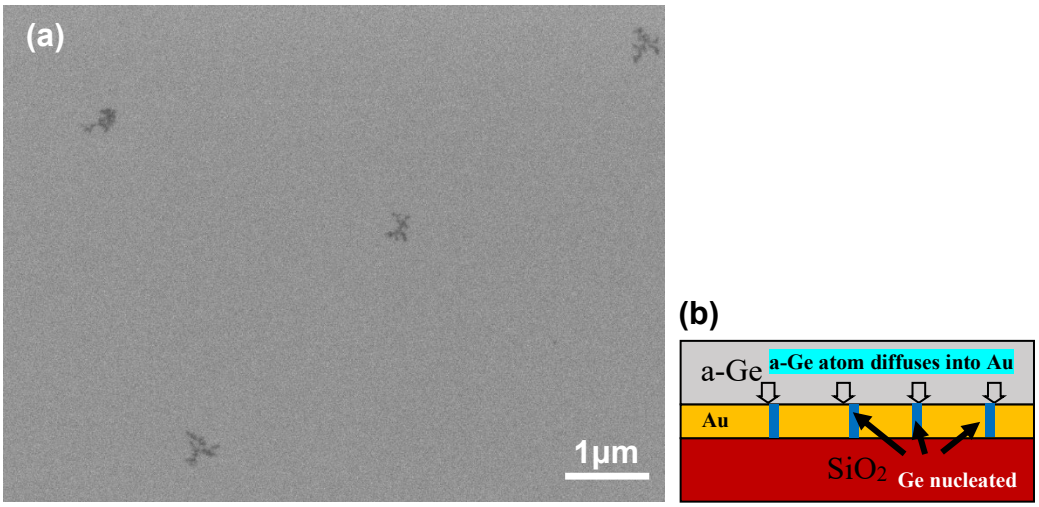

Fig. 4.4. (a) SEM image of Au(29nm)/Ge(46nm) after annealing at 140°C, (b) schematic illustration of the cross section after annealing at 140°C.

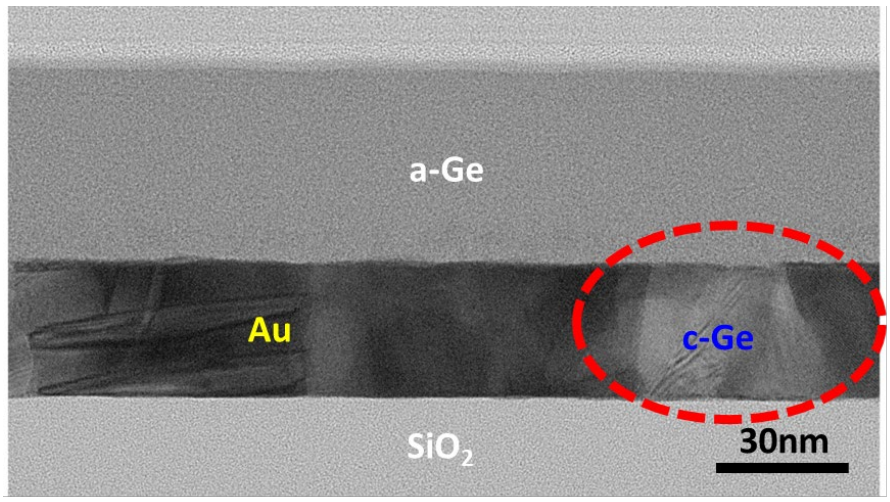

Fig. 4.5. Cross-sectional TEM image of Au(29nm)/Ge(46nm) after annealing at 140°C.

Fig. 4.6 shows the SEM image taken after annealing at 150°C. It is seen that crystalline Ge grain has grown larger compared to that after the annealing at 140°C (Fig. 4.4). This implies that during the annealing process, the Ge atoms are supplied to the nuclei through Au, which induces Ge lateral growth inside the Au layer. This growth mechanism will account for the thickness of the c-Ge layer which is close to the original Au layer. The growth of c-Ge proceeds in the similar fashion up to 180°C as shown in Fig. 4.6 to Fig. 4.9 (150°C to 180°C).

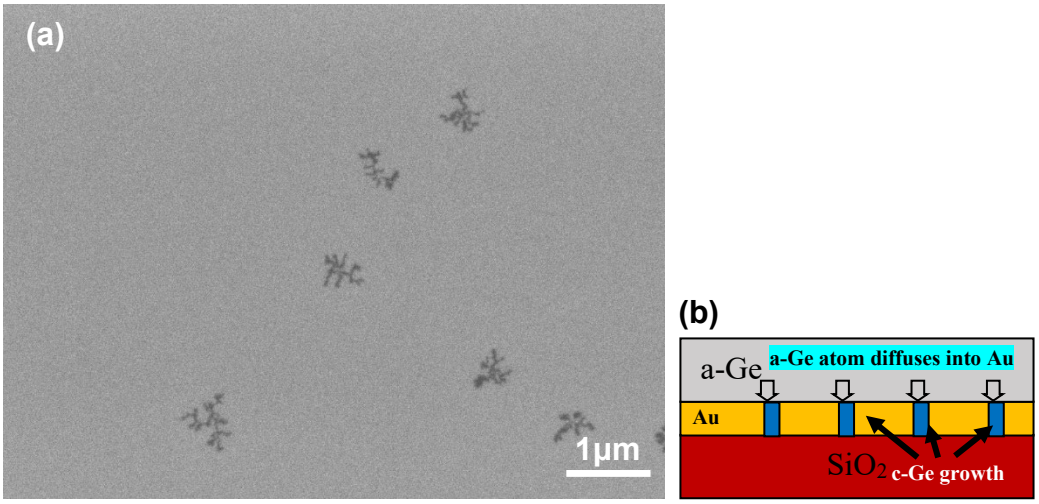

Fig. 4.6. (a) SEM image of Au(29nm)/Ge(46nm) after annealing at 150°C, (b) schematic illustration of the cross section after annealing at 150°C.

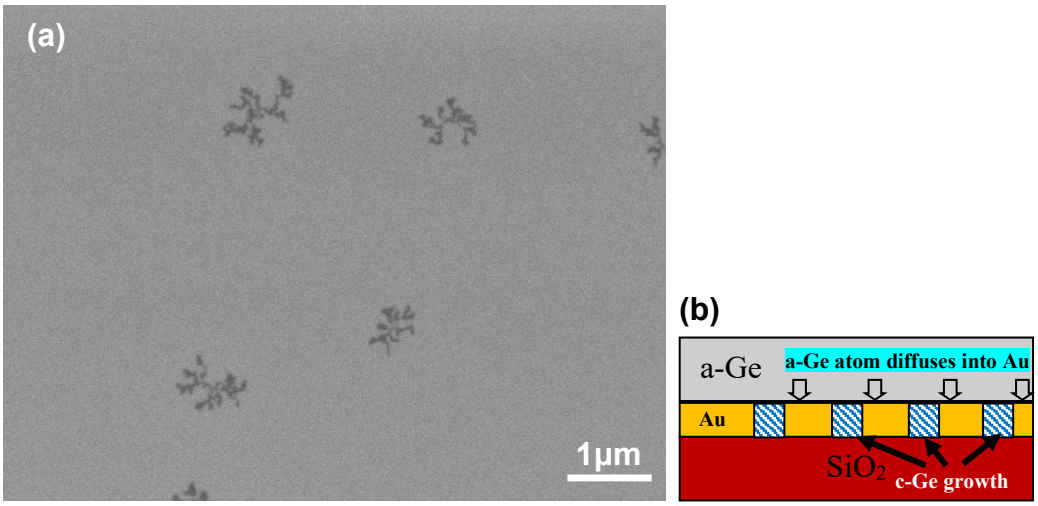

Fig. 4.7. (a) SEM image of Au(29nm)/Ge(46nm) after annealing at 160°C, (b) schematic illustration of the cross section after annealing at 160°C.

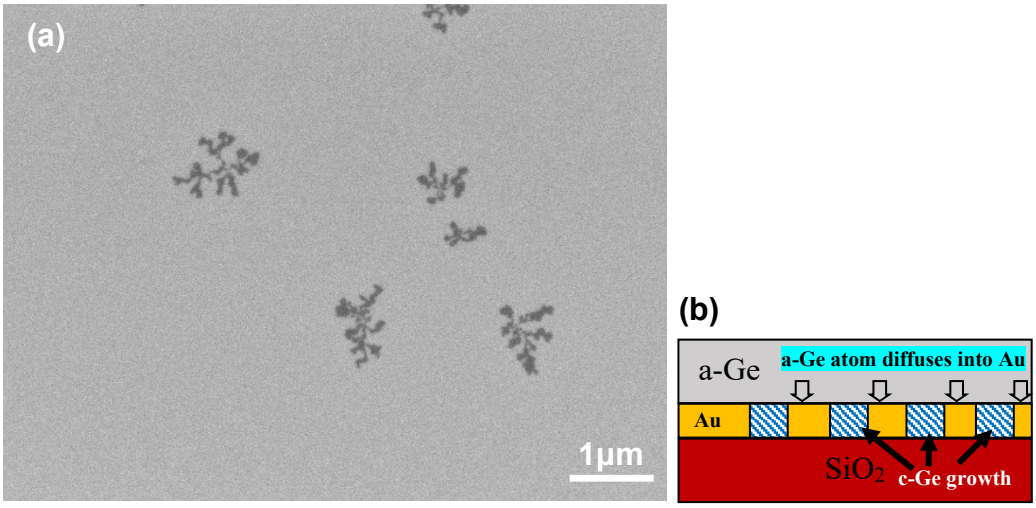

Fig. 4.8. (a) SEM image of Au(29nm)/Ge(46nm) after annealing at 170°C, (b) schematic illustration of the cross section after annealing at 170°C.

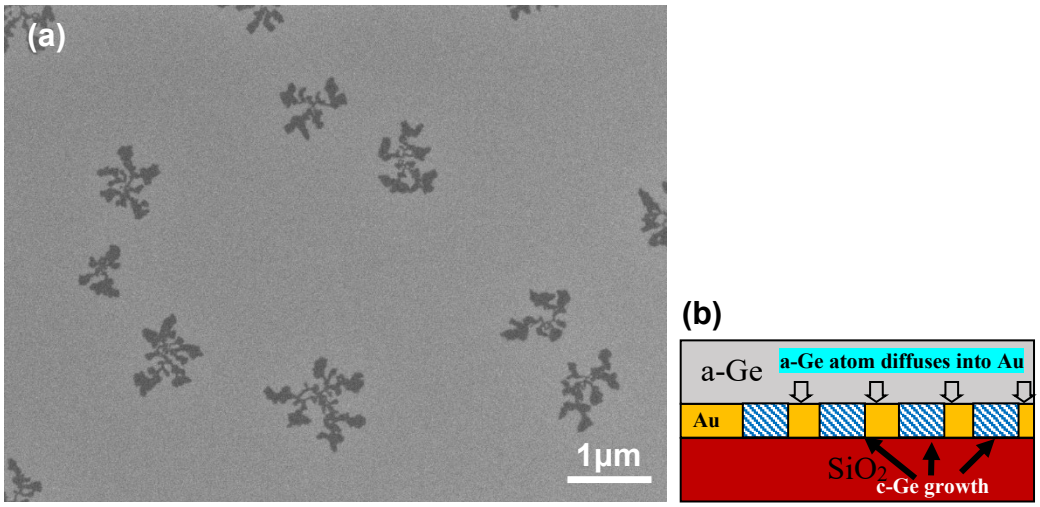

Fig. 4.9. (a) SEM image of Au(29nm)/Ge(46nm) after annealing at 180°C, (b) schematic illustration of the cross section after annealing at 180°C.

After the annealing temperature had reached 190°C, small white dots appear at the crystallized area as shown in Fig. 4.10. This implies that Au starts to move upward to the surface region, because of the lateral growth of crystalline Ge. This produces the stress to the Au region, and push up the Au layer, which is called a push-up phenomenon. The EDS spectra in Fig. 4.10(d) shows that a higher Au intensity is observed in the reacted area. This suggests that Au is indeed pushed up to the surface at the position where the nucleation of crystalline Ge has occurred.

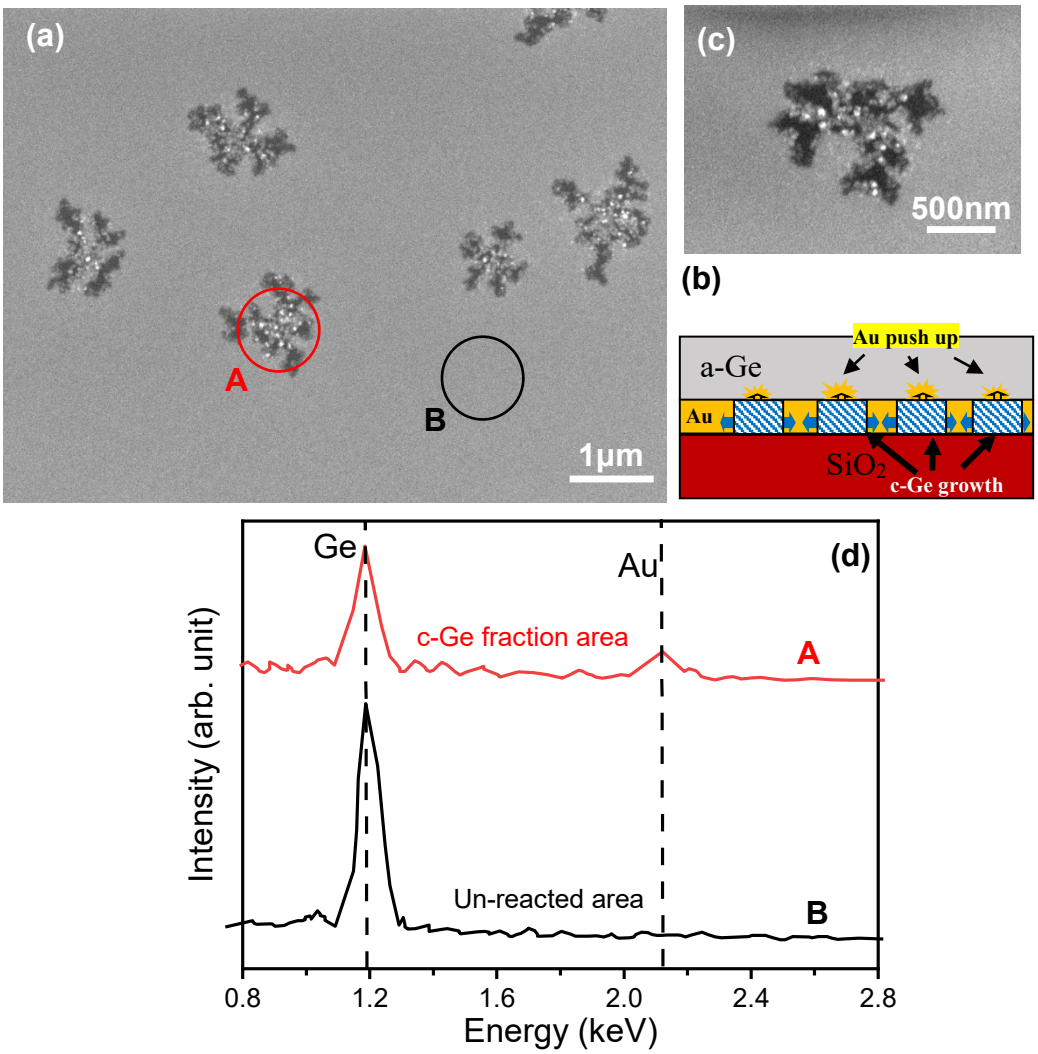

Fig. 4.10. (a) SEM image of Au(29nm)/Ge(46nm) after annealing at 190°C, (b) schematic illustration of the cross section after annealing at 190°C, (c) magnified SEM image after annealing at 190°C and (d) EDS spectra obtained at un-reacted and reacted areas after annealing at 190°C.

The SEM image of the sample after annealing at a temperature of 195°C is shown in Fig. 4.11. As the white area increases at the reacted area, it can be seen that small black dots appear at the same area. This implies a further push-up of the Au layer and a nucleation of c-Ge, 2nd layer, on the 1st c-Ge layer. The cross-sectional TEM image of this sample, Fig. 4.12, clearly shows the formation of the 1st and 2nd layers of c-Ge and the push up of the Au layer. It is clearly seen that the 1st layer grows with uniform thickness inside the original Au layer. The formation of 2nd layer could have been caused by the residual Ge during the Au push up.

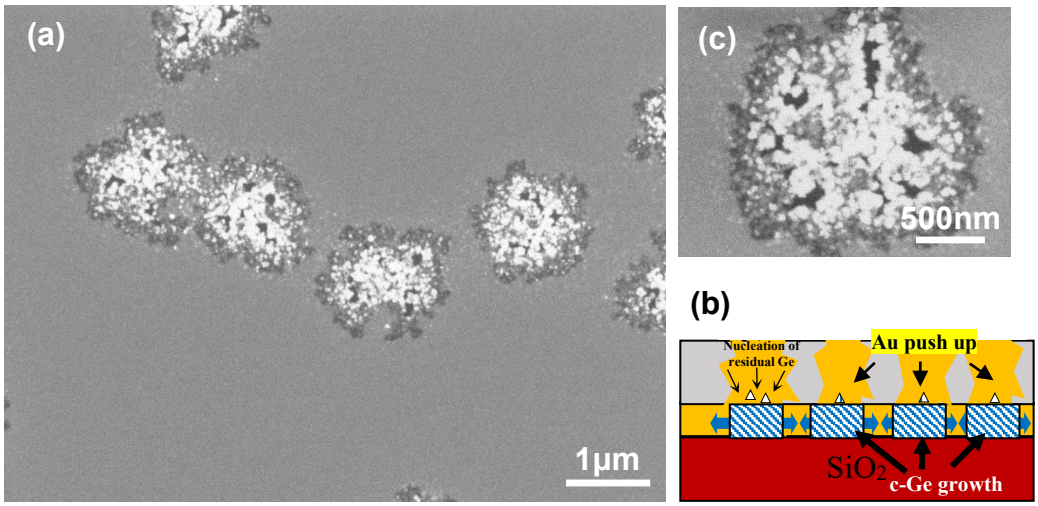

Fig. 4.11. (a) SEM image of Au(29nm)/Ge(46nm) after annealing at 195°C, (b) schematic illustration of the cross section after annealing at 195°C and (c) magnified SEM image after annealing at 195°C.

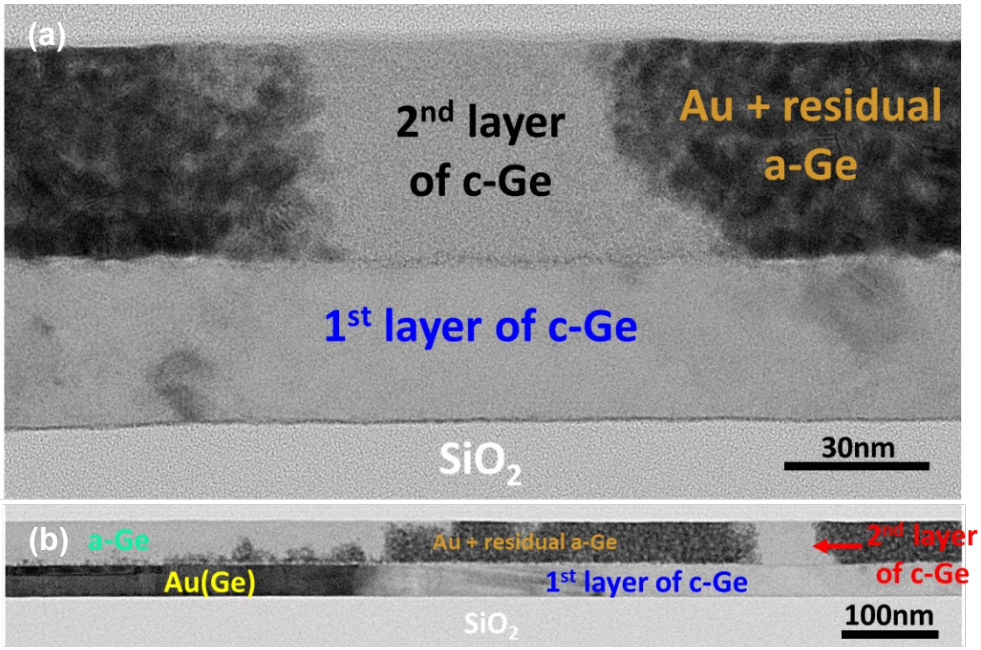

Fig. 4.12. Cross-sectional TEM image of Au(29nm)/Ge(46nm) after annealing at 195°C. (a) high magnification and (b) low magnification.

The SEM image of the sample annealed at 200°C is shown in Fig. 4.13. It can be seen that the reaction proceeds and the reacted areas are connected. The gray area seems to be the bilayer of pushed-up Au and c-Ge. The dark dot is likely to be the bilayer of the first and second layer of c-Ge. The bright area is the bilayer of the pushed-up Au and original Au layer. This region would be a hole in the first Ge layer after the etching process.

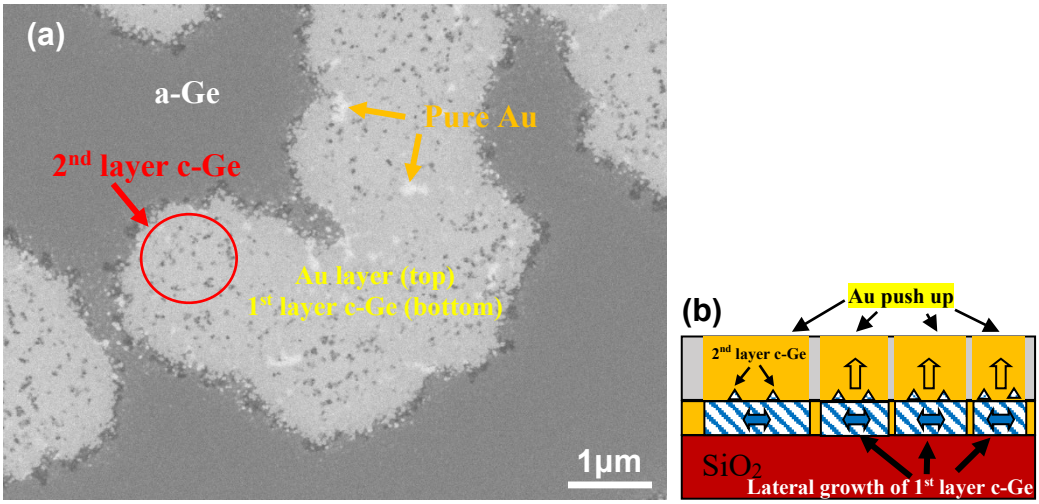

Fig. 4.13. (a) SEM image of Au(29nm)/Ge(46nm) after annealing at 200°C, (b) schematic illustration of the cross section after annealing at 200°C.

After the annealing temperature has reached 210°C, Fig. 4.14, the first layer of c-Ge spreads all over the surface and the Au region exist at the grain boundary. The SEM image at 210°C, Fig. 4.15, looks almost the same, which suggests that the reaction has already completed at this temperature. The film consists of the first crystalline Ge layer, whose thickness is the same as the original Au layer, and the second crystalline Ge layer formed on top of the first layer.

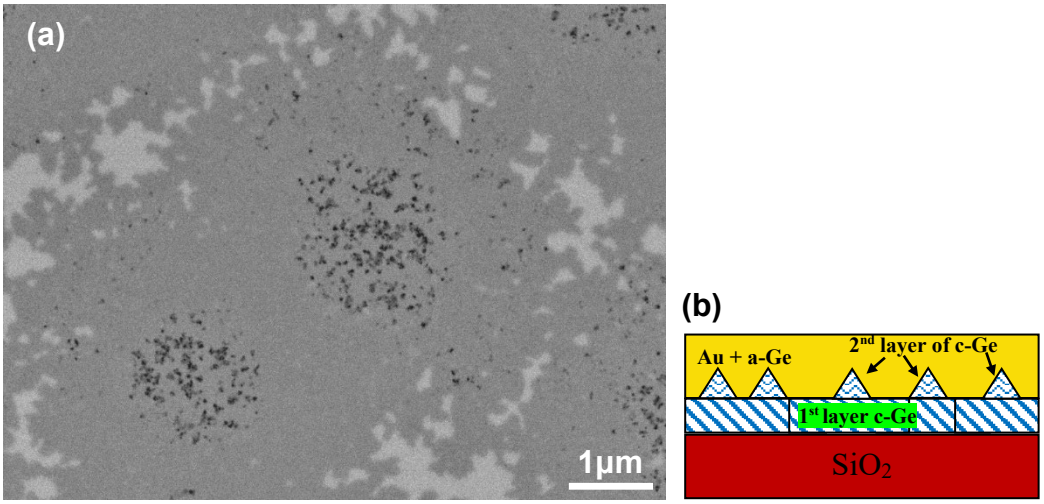

Fig. 4.14. (a) SEM image of Au(29nm)/Ge(46nm) after annealing at 210°C, (b) schematic illustration of the cross section after annealing at 210°C.

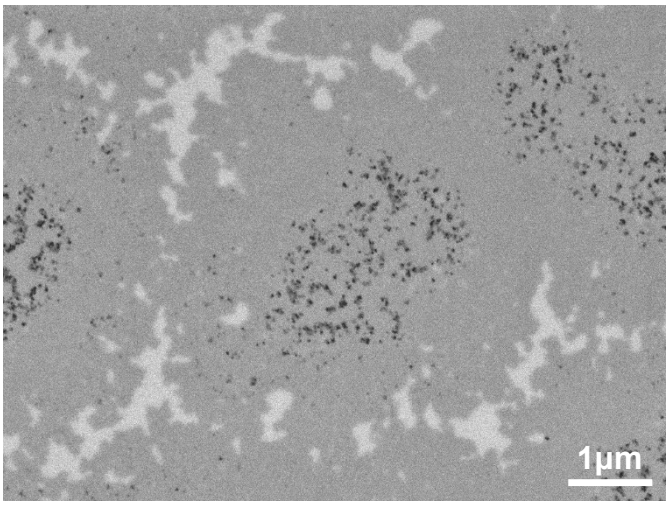

Fig. 4.15. SEM image of Au(29nm)/Ge(46nm) after annealing at 220°C.

4.3.2 Investigation of the formation of 1st and 2nd layers of crystalline Ge films.

Figure 4.16 shows the magnified SEM images of the Au(29nm)/Ge(46nm) sample after annealing at temperatures ranging from 155°C to175°C. A small amount of 2nd layer of crystalline Ge has been observed after annealing at 155°C. To look at the evolution of the 1st and 2nd layer growth, the coverage of the 1st and 2nd layers of c-Ge obtained from the SEM images in Fig. 4.16 was analyzed by ImageJ program and plotted in Fig. 4.17. It is clearly seen that the coverage of the 1st layer of crystalline Ge increases rapidly at ~165°C and approaches ~100% at 175°C. On the other hand, the formation of the 2nd layer is much slower and saturates at ~20% at ~170°C. This implies a different growth

mechanism for the second layer. As will be discussed in the next section, some amount of Au could diffuse into the a-Ge layer. This could induce Ge crystallization without layer exchange and a poor crystal quality as shown in the previous chapter. The different growth temperature for the first and second layer could be used to suppress the formation of the 2nd layer and promotes the formation of a smooth surface as will be discussed in the next chapter.

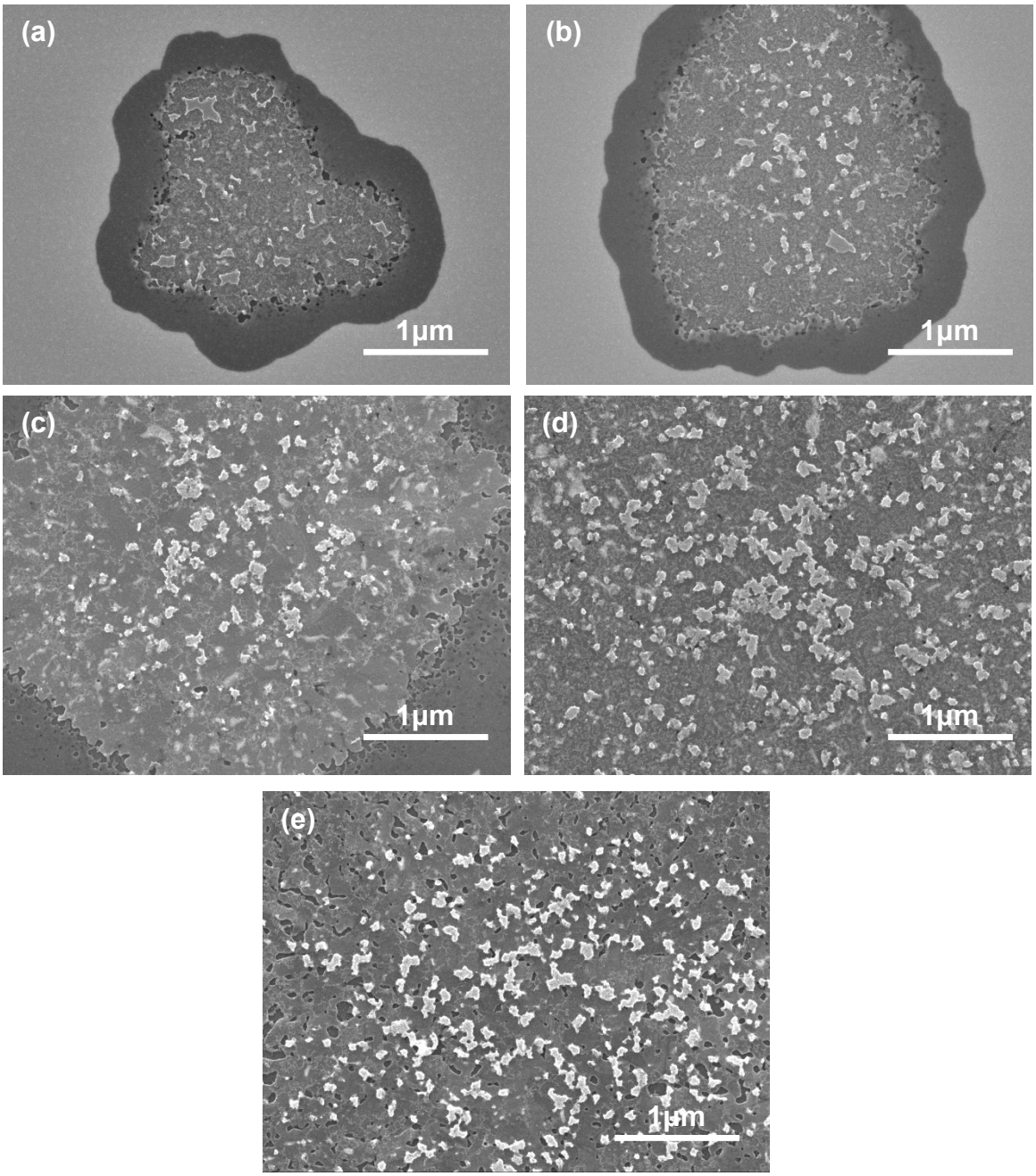

Fig. 4.16. Magnified SEM images of Ge films annealed at (a) 155°C, (b) 160°C, (c) 165°C, (d) 170°C and (e) 175°C. The Au layer is removed by wet etching process.

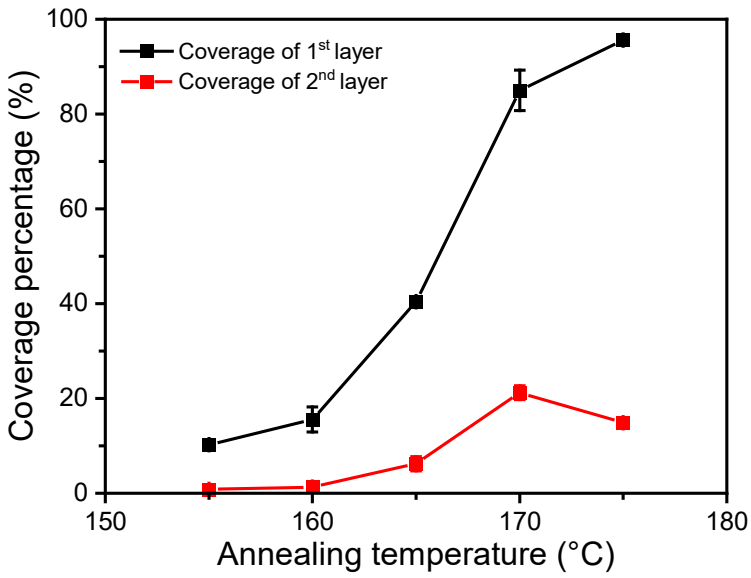

Fig. 4.17. Evolution of the coverage of 1st and 2nd layers of crystalline Ge of Au(29nm)/Ge(46nm) sample.

4.3.3 Influence of Au and Ge layer thickness on the formation of crystalline Ge

The growth of crystalline Ge is directly affected by both the initial Au and Ge layer thicknesses. In the previous chapter, we have shown that the Au layer thickness affects crystal orientation. Additionally, the initial a-Ge thickness affects crystal morphology. Based on these new findings in the previous section, the crystallization mechanism is discussed in terms of the Au layer thickness and a-Ge layer thickness.

4.3.3.1 Effect of Au thickness

Figure 4.18 shows the schematic for the crystallization process of Ge film when the initial Au layer is thin. The Ge diffusion into the Au layer is blocked at the Au/SiO_2 interface and the Ge density near the SiO_2 surface could be larger than that near the a-Ge/Au interface. Furthermore, the SiO_2 surface could promote heterogeneous nucleation of Ge crystals. These factors could lead to lower crystallization temperature and higher nucleation rates for samples with thinner Au layers. This will lead to higher c-Ge grain density. Moreover, when the Au is thin, the Au/SiO_2 interface is likely to promote Ge crystal to orient in the (111) direction to minimize the interfacial energy between crystalline Ge and the SiO_2 surface.

In the case of a thick Au sample, Fig. 4.19, Ge concentration should be larger near the a-Ge/Au interface in the Au layer than near the Au/SiO_2 interface. Therefore,

nucleation of crystalline Ge is likely to occur near the a-Ge/Au interface. The crystal orientation was random for samples with thicker Au layers in the present study, which implies that the anisotropy in the interface energy between Au and c-Ge is small [1]. Moreover, the larger Au thickness could lead to the lower Ge density and lower nucleation rate of c-Ge. This could account for the lower c-Ge island density and dendritic shape of the island.

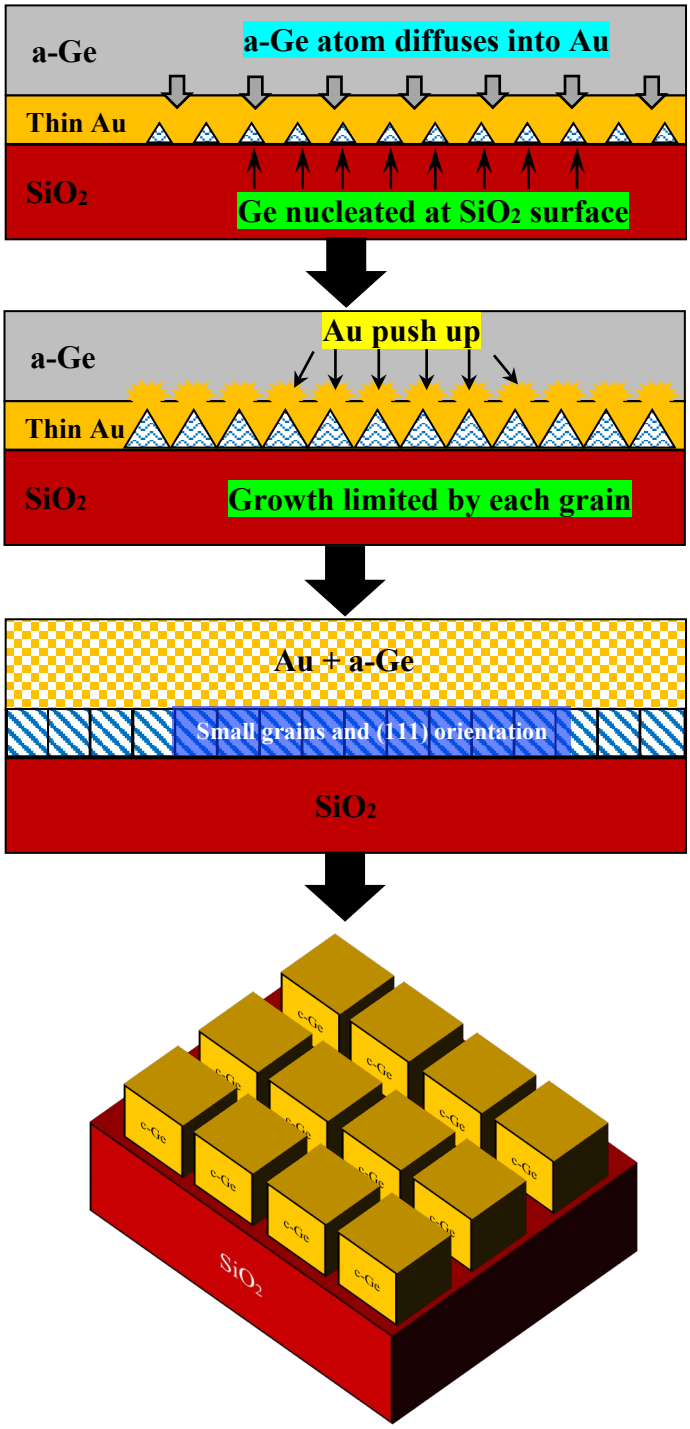

Fig. 4.18. Schematic of the growth model for thin Au catalyst.

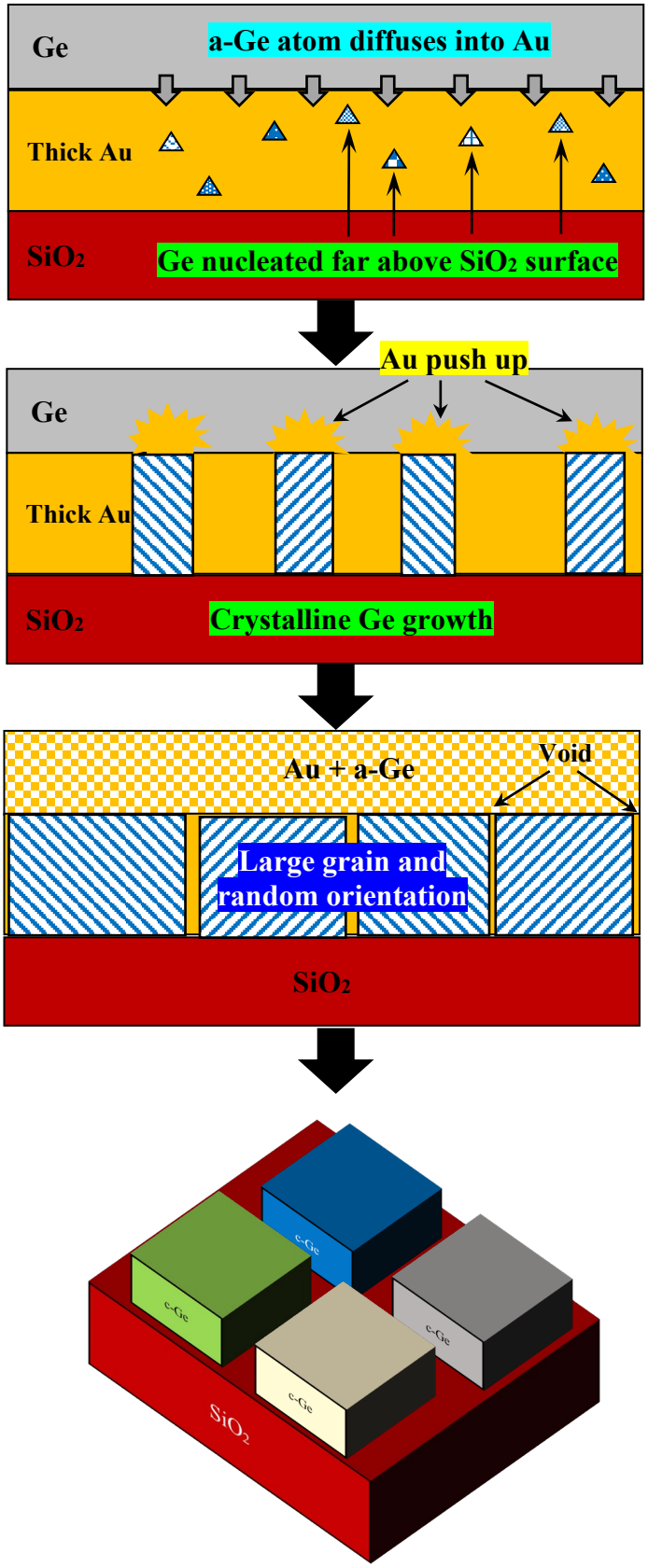

Fig. 4.19. Schematic of the growth model for thick Au catalyst

4.3.3.2 Effect of Ge thickness

The crystal morphology is greatly affected by the influence of Ge layer thickness as seen in the previous chapter. Figure 4.20 shows the schematic illustration of the Ge crystallization process when the initial a-Ge is thin. First, Ge diffuses into the Au layer during the annealing process to form an alloy. At some Ge concentration, c-Ge will nucleate by phase separation because Au/Ge is a eutectic system. Since the amount of a-Ge is not enough to complete the first layer, crystalline Ge remain as isolated islands without the 2nd c-Ge layer.

When the initial a-Ge has an appropriate thickness, Fig. 4.21, the c-Ge grains connect with each other and the first layer is almost complete. Some of the residual Ge left in the upper layer crystallizes to form the second layer.

When the initial a-Ge layer is thicker, Fig. 4.22, the higher Ge concentration in the upper layer could promote nucleation of the second layer. As a result, Ge necessary to complete the first layer is not supplied to the bottom layer and the void will appear.

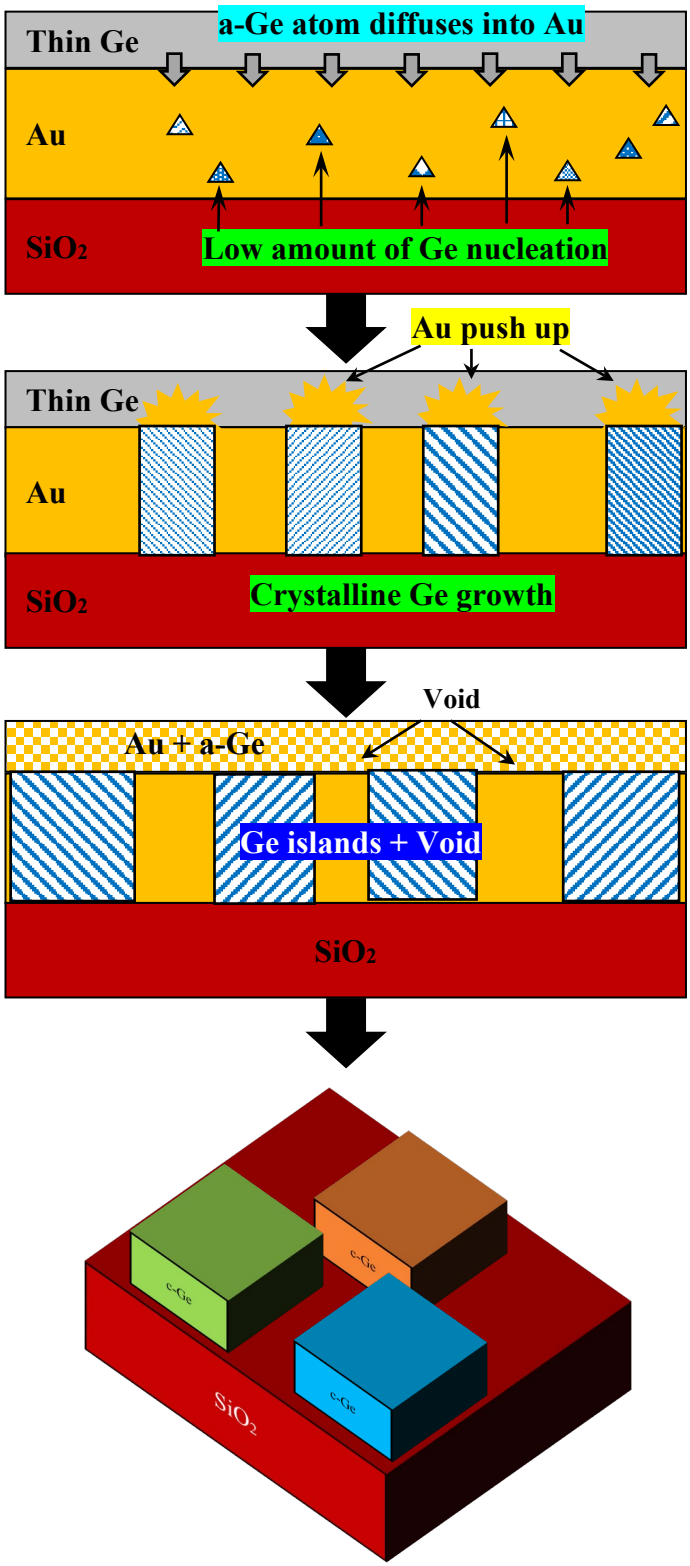

Fig. 4.20. Illustration model for the growth process of Ge crystallization by thin initial a-Ge.

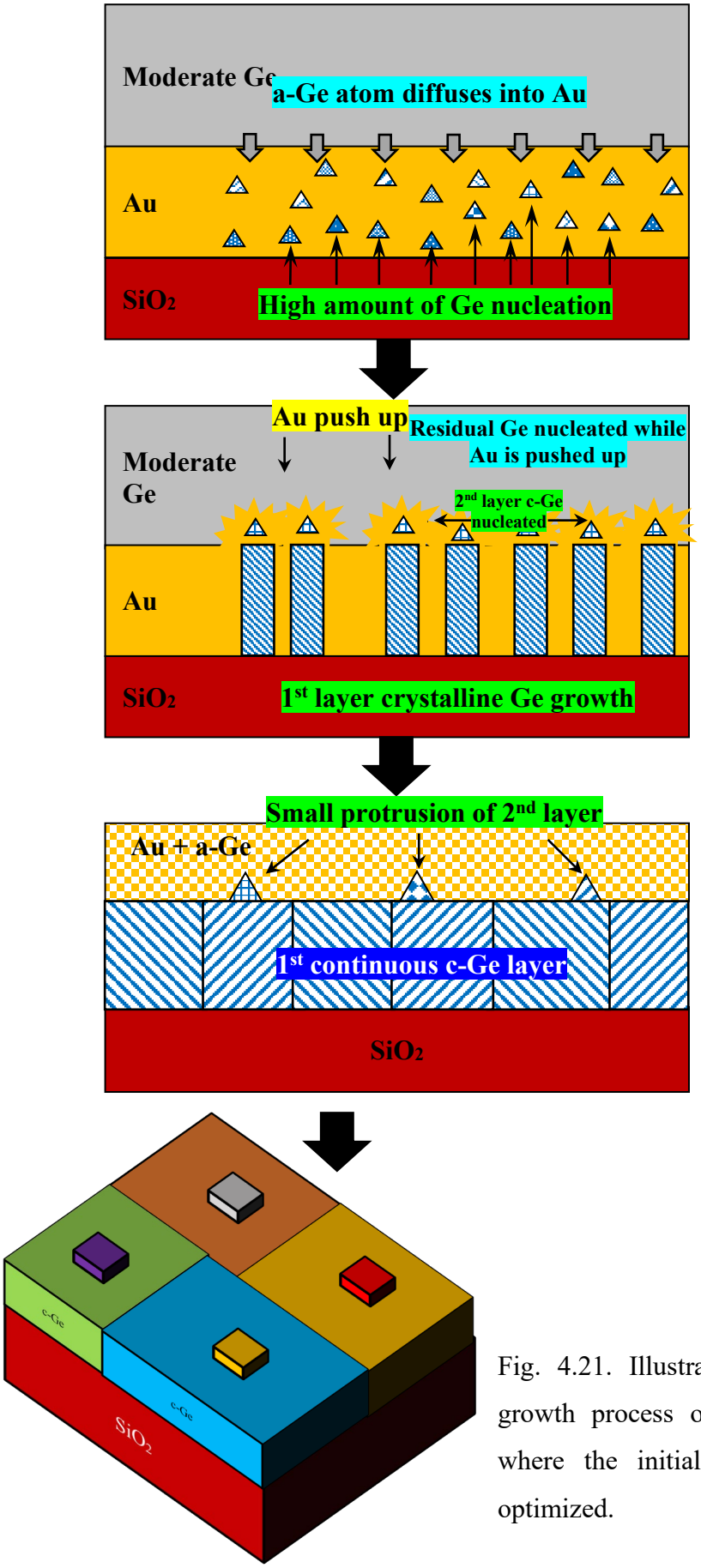

Fig. 4.21. Illustration model for the growth process of Ge crystallization where the initial a-Ge thickness is optimized.

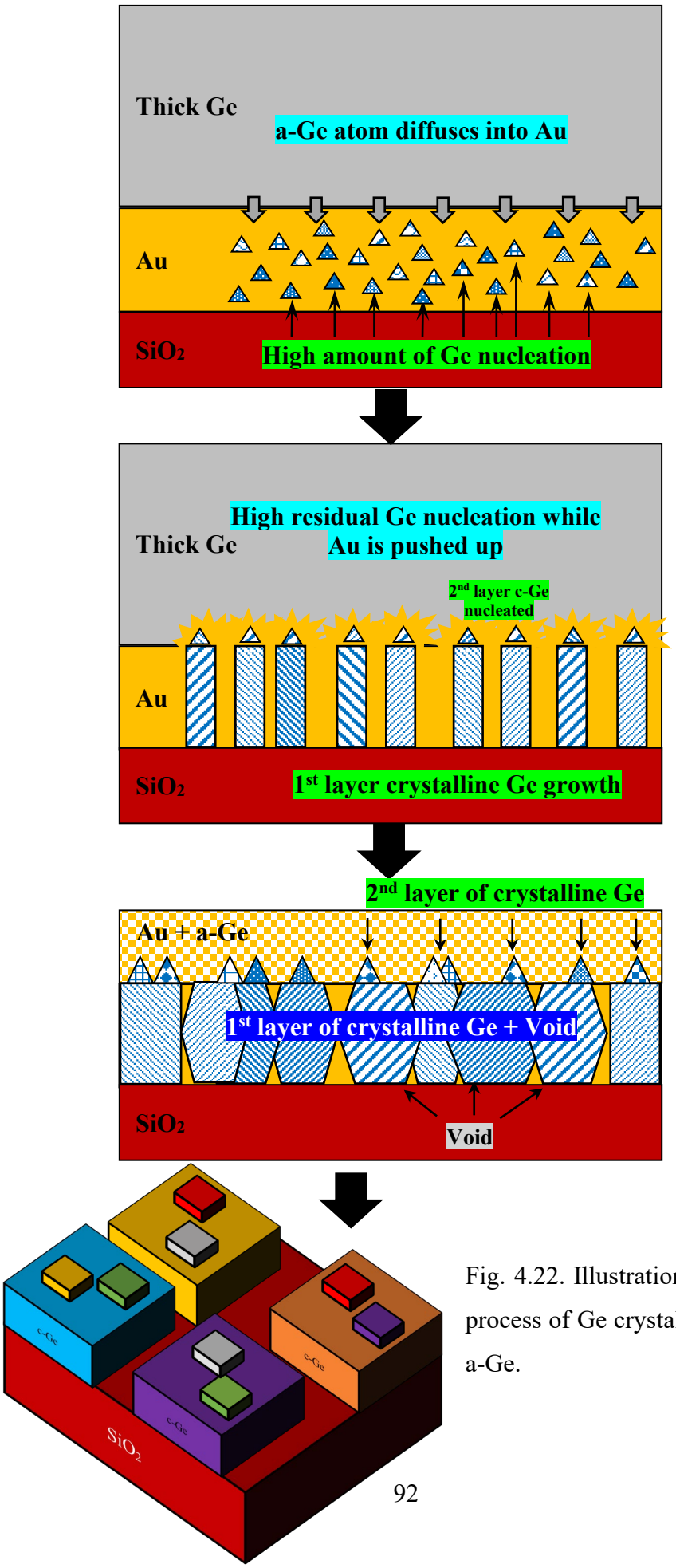

Fig. 4.22. Illustration model for the growth process of Ge crystallization by thick initial a-Ge.

Au/Ge is a eutectic system and the eutectic temperature is 361°C as shown in the phase diagram in Fig. 4.23 [2]. The composition at the eutectic point is 28 at.% Ge and the solubility of Ge in Au is 3 at.% which decreases as the temperature decreases.

In the layer-exchange type crystallization, crystallization of Ge thin films occurs in the Au layer. Konno and Sinclair conducted ex and in-situ cross-section transmission electron microscopy experiments on the Al/Si bilayer [3, 4]. They demonstrated that when an Al/a-Si multilayer structure is heated to 200°C, crystalline Si nuclei develop within the Al layers, followed by the dissociation of a-Si layer.

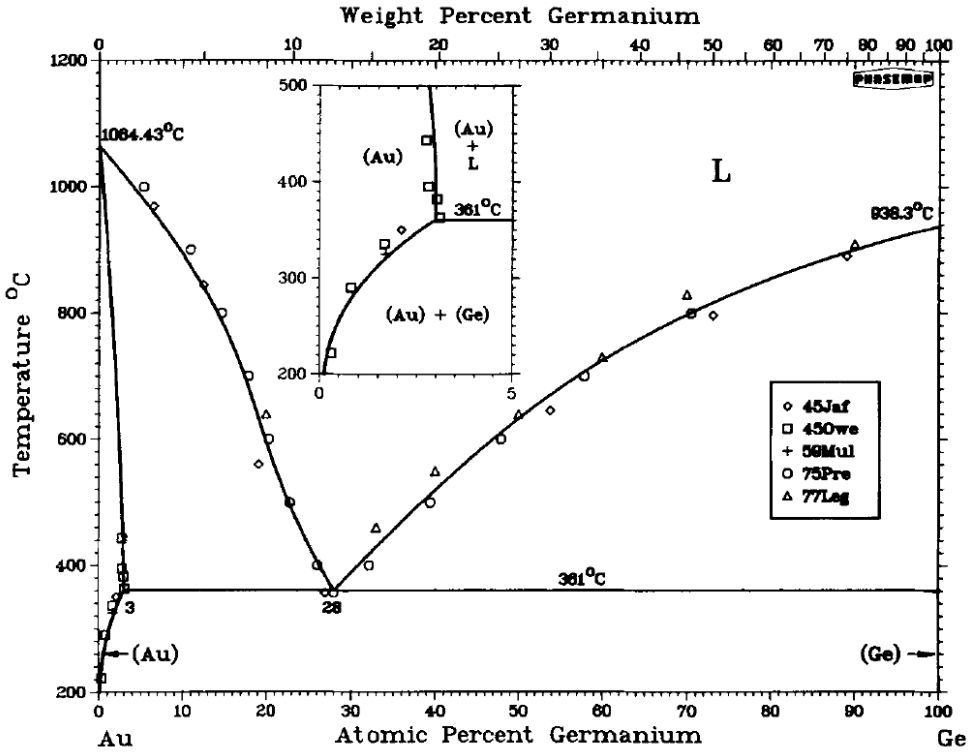

Fig. 4.23. Phase diagram of Au/Ge eutectic system [2].

In the Au/Ge system, nucleation of crystalline Ge in Au nanoparticle has been observed at a temperature as low as 150°C. An existence of a very thin supercooled liquid alloy layer surrounding a solid particle is proposed [5]. Y. Wakabayashi et al.[6], found that the Ge atoms diffuse immediately into Au even at room temperature, which contrasts with the fact that the solubility of Ge in Au is very small at room temperature. These phenomena seem to imply the weakening of the bonding strength between Au atoms by Ge incorporation.

Figure 4.24 from Ref. [6] depicts the Gibbs free energy curves of fcc (G_{fcc}), diamond ($G_{diamond}$), and liquid phases (G_{liquid}) of an AuGe system at room temperature (27°C). The free energy is expressed by line a in Fig. 4.24(a), which is a common tangent of G_{fcc} and $G_{diamond}$ when the fcc and diamond phases coexist. Ge's solubility in Au is estimated to be 8×10^{-5}%. The common tangent of these calculated free energies reproduces the available experimental values of solid solubility of 0.30% and 0.81% at 220°C and 290°C [2], respectively. Because the free energy of an amorphous structure is 0.15 eV/atom higher than that of a crystal [7], the free energy curve of an amorphous structure ($G_{\mathrm{amorphous}}$) should be higher than that of a diamond phase ($G_{diamond}$) by this amount. As a result, when an amorphous phase coexists with a fcc phase, the system's free energy is expressed by line b. This raises the solubility limit to 2.6×10^{-2}%, as illustrated in the magnified plot in Fig. 4.24(b). The surface and interface energies are taken into account, as shown in the insets of Fig. 4.24(b). It is assumed that the deposited Ge atoms exist as an amorphous film (a-Ge) on the Au film in the phase-separated state (right inset). As a result, the surface energy of a-Ge (γ_{a-Ge}) and the interface energy between a-Ge and Au ($\gamma_{a-Ge/Au}$) must be considered. When Ge is completely dissolved in Au (left inset), only the surface energy of Au (γ_{Au}) is taken into account. As a result, the following equations express the difference in free energy ($\triangle G$) between the phase-separated state (right inset) and the fully dissolved single fcc phase (left inset):

$$\triangle G = G_{\mathrm{fcc}} - \left(x_{Ge}G_{\mathrm{amorphous}} + x_{fcc}G_{\mathrm{fcc}}\right) - S \triangle \gamma / n_{AuGe}, \quad (1)$$

$$\triangle \gamma = \gamma_{a-Ge/Au} + \gamma_{a-Ge} - \gamma_{Au}. \quad (2)$$

where x_{Ge} and x_{fcc} are the molar fractions of the Ge and fcc phases, respectively. The difference in surface and/or interface energies of the two states is defined as $\triangle \gamma$ in Eq. (2). S denotes the surface area, and n_{AuGe} denotes the total molar quantity of Au and Ge which exist below this surface area. Because n_{AuGe} is roughly proportional to the thickness of the Au film, the final term in Eq. (1) is inversely proportional to the thickness of the Au film and will be negligible for a bulk material.

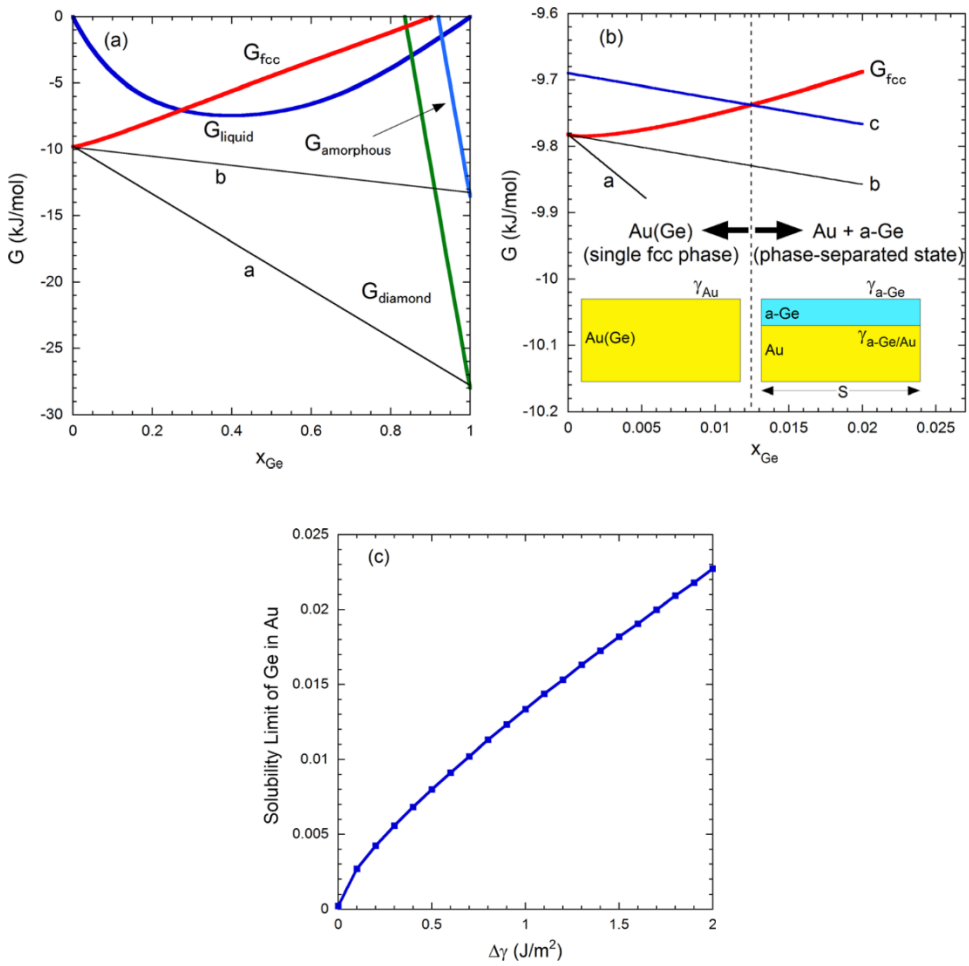

Fig. 4.24. (a) Calculated Gibbs free energy of fcc, diamond, amorphous, and liquid phases as a function of Ge content. (b) Magnified view (a) near x_{Ge} ~ 0. (c) $\triangle\gamma$ dependence of the solubility limit [47].

If the values in Ref. [8] are used for the surface and interface energies, $\triangle\gamma$ is calculated to be 0.91 J/m^2. As a result, the free energy of the separated state should be greater than line b by $S\triangle\gamma/n_{AuGe}$, which corresponds to line c in Fig. 4.24(b). Line c and G_{fcc} cross at x_{Ge} ~0.013, indicating that $\triangle G$ in Eq. (1) is negative and that a single fcc phase is more stable than a phase-separated state below this limit. At room temperature, a fcc phase can accommodate up to 1.3% of Ge, which is much higher than the solubility limit of an equilibrium AuGe system. Because the surface and interface energies are uncertain [8], the solubility limit as a function of $\triangle\gamma$ is plotted in Fig. 4.24(c). Over a wide range of $\triangle\gamma$, a solubility limit of more than ~0.1% is satisfied,

implying that the increase in solubility could be explained by the manifestation of the interface energy in the thin-film structure.

In the layer-exchange type MIC of Au/Ge, Ge atoms are expected to diffuse into the Au layer from the a-Ge layer. The concentration of Ge in the Au layer approaches the equilibrium value which is specified by the tangent point of line b and G_{fcc} in Fig.4.24(b). Nevertheless, since this concentration is larger than the equilibrium value between c-Ge and Au, the alloy will phase separate into c-Ge and Au at some Ge concentration. Once the nucleation of c-Ge occurs, the grain will grow laterally by absorbing the Ge atoms supplied through the Au layer. As the c-Ge layer occupies the bottom layer, Au will be pushed up to the top layer to complete layer exchange.

The overall driving force behind the crystallization process mentioned above is the reduction of Gibbs free energy by the transformation of a-Ge to c-Ge (0.15 eV/atom) [7]. However, the transformation from amorphous to crystalline phase by SPC requires quite a high temperature and long annealing time because of the strong Ge-Ge covalent bond. The activation energy for crystallization is reported to be 3.8 eV [9]. In contrast, the crystallization of a-Ge by Au-induced crystallization takes place at a lower temperature, and a much smaller activation energy of 1.8 eV is reported [9]. This is probably due to the lower activation energy of either the dissolution process of Ge into Au or the attachment process of the dissolved Ge atoms to c-Ge.

The reduction of activation energy for dissolution was explained in the *interstitial model* by Tu [10]. The model is based on the initial intermixing of metal and Si atoms at the interface, and it is proposed that the metal atoms jump into Si, forming metal interstitials. These Si interstitial defects are expected to significantly alter the nature of the neighboring Si-Si bonds. The covalent bonds will no longer be locally confined. As a result, the metal interstitial induces the conversion of the neighboring covalent Si-Si bond to a non-covalent bond. This modified bond is weaker than a saturated covalent bond. Tu [10] contends that Si atoms can dissociate from the lattice at a lower activation energy and diffuse into the metal. The interstitial model was also used to explain the crystallization process in Au/Si [11] and Al/Si [12] systems.

Au/Ge system is also used in the Ge nanowire growth. It is known that the AuGe alloy nanodot exists on top of the c-Ge nanowire and Ge is supplied from the alloy to the nanowire for further growth. This process occurs at a temperature as low as 150°C which

implies a low activation energy for the attachment of Ge atoms from the alloy to c-Ge [13]. Considering the facts that this temperature is close to the crystallization temperature in this study and some amount of Ge can diffuse into Au even at room temperature [6], the attachment of Ge atoms in Au to the c-Ge phase seems to be the rate limiting step and the activation energy of 1.8 eV obtained in Ref. [9] might correspond to this process.

Two metastable phases, β and γ-AuGe, are reported as the possible phases for the AuGe nanodot on c-Ge nanowire. Although the γ phase has a bct structure with a rather large Ge concentration (40-50 at.%), β phase has a hcp structure with a rather broad concentration range (3-25 at.%). The XRD peaks for the fcc (111) and hcp (001) diffraction are likely to appear at a close position and the rapid decrease of the Au (111) intensity could be explained by the appearance of the β-phase which promotes the attachment of Ge atoms dissolved in Au to the c-Ge phase.

4.4 Conclusion

In this chapter, we investigated the growth mechanism of Ge thin films crystallized by Au-induced layer exchange process. The crystallization process has been investigated by in-situ XRD, ex-situ SEM and TEM observations. The results show that the nucleation of c-Ge occurs mainly inside the bottom Au layer. The c-Ge grows laterally and the Au is pushed-up to complete layer exchange. It is also found that the excess Ge forms the second c-Ge layer on the first layer and the growth of the second layer occurs at a higher temperature compared to the first layer. This behavior can be used to suppress the growth of the second layer and decrease the surface roughness, which will be discussed in detail in the next chapter.

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Chapter 5

Formation of a continuous c-Ge layer by controlling the annealing condition

5.1 Introduction

In the last chapter, it was found that the c-Ge layer crystallized by Au without an insert layer has a double layer structure which was also observed for c-Ge films obtained by Al-induced crystallization with an insert layer. It was also found that the second layer starts to nucleate at a higher temperature compared to the first layer. This implies that it might be possible to induce only the growth of the first layer, which has a higher crystal quality, by choosing an appropriate annealing temperature.

First, a heating rate effect on the crystallization behavior has been investigated. It was found that a better crystal quality is achieved for lower heating rate which supports the assumption that the growth of the second layer can be suppressed by choosing an appropriate annealing temperature. By also reducing an Au layer thickness, a very smooth and continuous (111) oriented c-Ge layer which only consists of a first layer is achieved by annealing a Au(10nm)/Ge(18nm) bilayer at 170°C for 1 hour. The temperature is much lower compared to that of the process using an insert layer. These findings will be useful for the fabrication of high-quality Ge thin films on various inexpensive flexible substrates as a seeding layer for next generation solar cell applications.

5.2 Experimental methods

In this experiment, Au film was used as a catalyst for Ge film crystallization. Si wafers with 100 nm thick thermally grown oxides were used as substrates. These substrates were cleaned by acetone and ethanol using an ultrasonic cleaning bath prior to the sputtering process. Au (target: 99.99%, deposition rate: 0.72 nm/s) layers are first deposited and a-Ge (target: 99.999%, deposition rate: 0.32 nm/s) layers are successively deposited on top of Au by RF magnetron sputtering process with Ar plasma (Ar gas purity 99.9999%, pressure during deposition: 3×10^{-3} Torr) to form an Au/Ge bilayer. The Au layer thickness is fixed at 29 nm, while the a-Ge layer thickness is also kept constant at 46 nm. The schematic structure of the film on SiO_2 substrate for this experiment is shown in Fig. 5.1. To crystallize Ge film by Au-induced layer exchange process, the Au/Ge bilayer was annealed by thermal annealing process under N_2 ambient at 220 and 250°C. The heating rate ranged from 0.5 to 10°C/min in order to examine the effect of heating rate. To look at the details of the crystallization process, in-situ x-ray diffraction (XRD) experiment are also performed in the θ-2θ mode with a scattering vector normal to the film surface using a built-in heating chamber under N_2 ambient with temperatures ranging from 100 to 300°C.

After selectively removing Au by a solution containing KI and I_2, the quality of Ge crystal was investigated by Raman spectroscopy with a 532-nm laser excitation. The surface morphology was observed by scanning electron microscope (SEM) and the coverage of crystalline Ge is analyzed by an ImageJ program. Electron backscatter diffraction (EBSD) measurement has been also performed to identify the crystal orientation. The electrical property was obtained by Hall effect measurement with van der Pauw method.

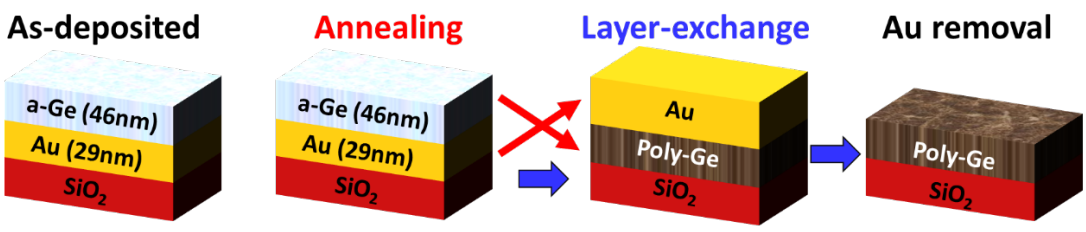

Fig. 5.1. Schematic structure of a-Ge/Au film on SiO_2 substrate for this experiment.

5.3 Results and discussion

5.3.1 Characterization of crystalline Ge by XRD measurement

The formation of crystalline Ge has been investigated by XRD measurement. Figures 5.2(a) and (b) show the XRD profiles of the samples after annealing at 220°C and 250°C, respectively. The Ge (111) diffraction peaks around 27.3º are clearly observed, which shows that Ge thin films are crystallized at this temperature.

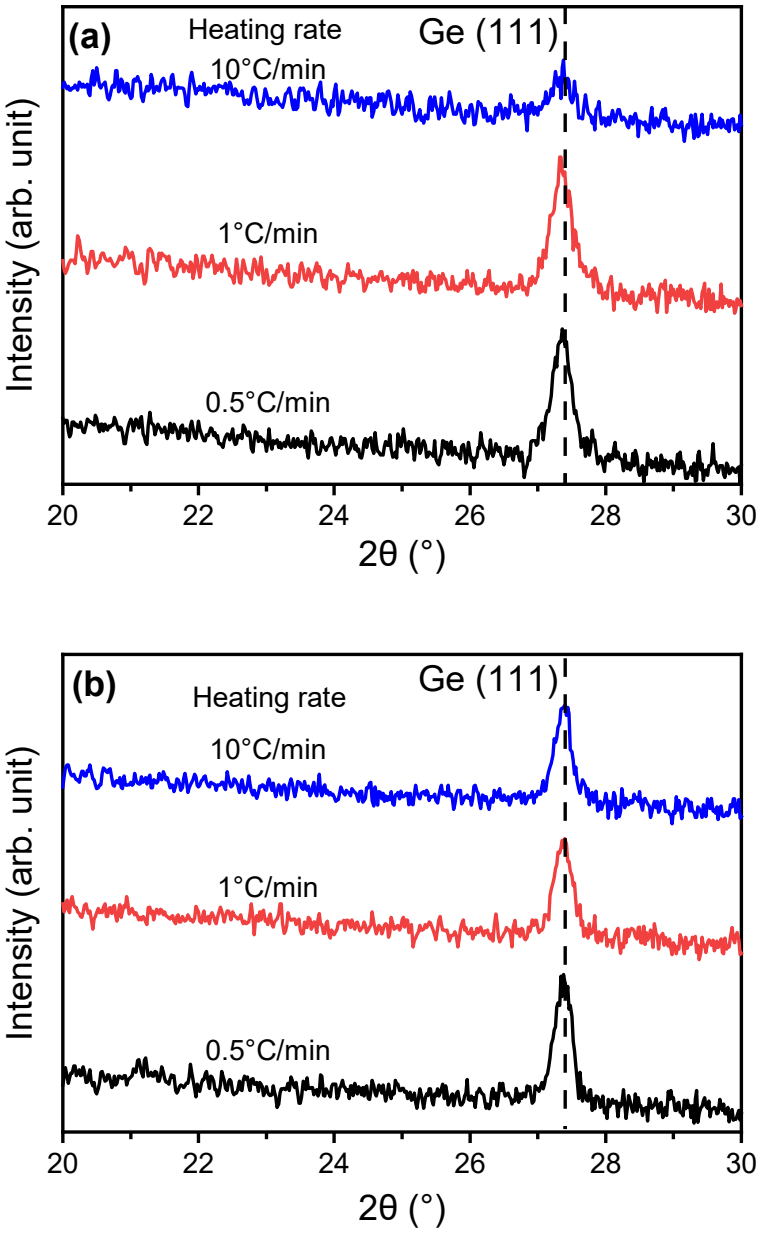

Fig. 5.2. XRD profiles of Ge films obtained after annealing at (a) 220°C and (b) 250°C for 1 hr.

5.3.2 Investigation of crystallization process by in-situ XRD observation

In-situ XRD was also performed to investigate the crystallization process of Ge film for both slow and fast heating rates. Figure 5.3 shows a dual axis plot of Ge (111) and Au (111) intensity obtained by in-situ XRD experiment. Figure 5.3(a) shows the evolution of Ge (111) and Au (111) intensity at a heating rate of 1°C/min. The Ge (111) intensity starts to appear at a temperature around ~165°C. The intensity increases rapidly up to ~175°C and increases gradually afterwards. It is seen that the Au(111) intensity decreases rapidly during the increase of Ge(111). Au (111) intensity increases again above 200°C. The result with a faster heating rate (10°C/min), Fig. 5.3(b), shows qualitatively the same behavior.

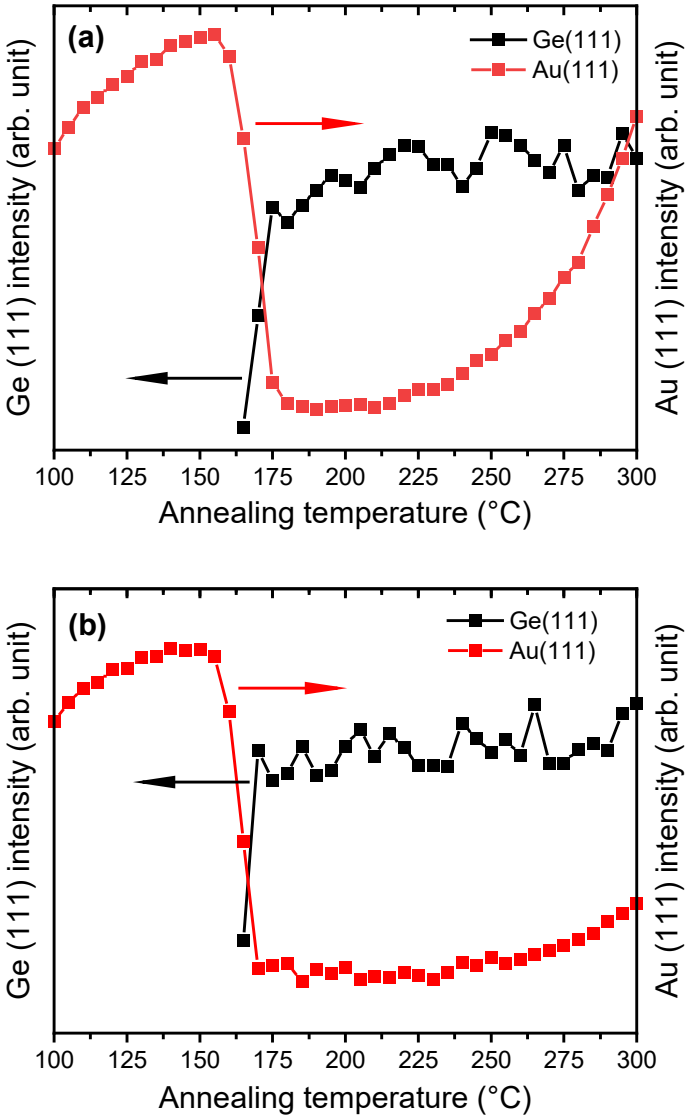

Fig. 5.3. Evolution of the Ge (111) and Au (111) diffraction intensity obtained by in-situ XRD measurement. The heating rates are (a) 1°C/min and (b) 10°C/min.

5.3.3 Crystal quality investigation by Raman measurement

The Raman measurement was also performed to determine the existence of crystalline Ge after annealing at several conditions. Au was removed by KI and I_2 solution before measurement. Figure 5.4 shows the Raman spectra of the Ge films after annealing at 220°C (Fig. 5.4(a)) and 250°C (Fig. 5.4(b)) with different heating rates. It is clearly observed that the peaks appear at around 300 cm^{-1} which shows the existence of crystalline Ge. These results are in accordance with the XRD results in Fig. 5.2.

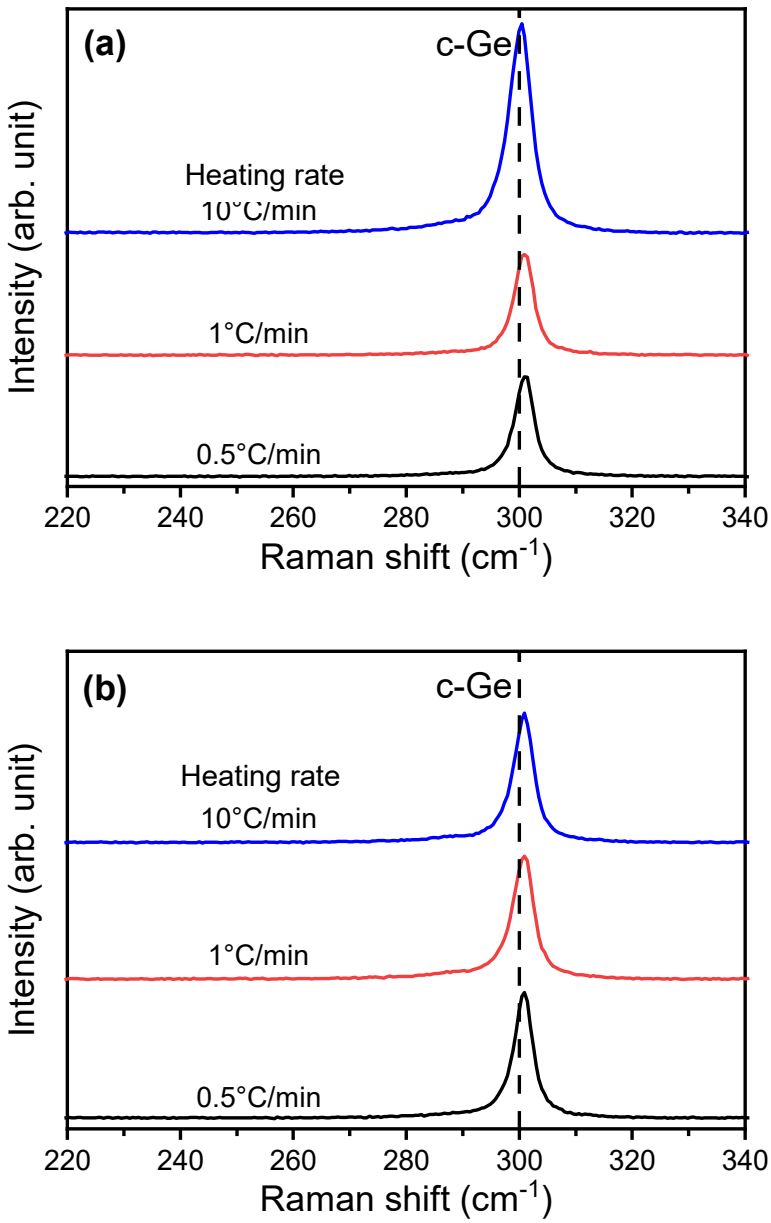

Fig. 5.4. Raman spectra of Ge films obtained after annealing at (a) 220°C and (b) 250°C for 1 hr.

To estimate the crystal quality of the Ge films, Raman shift and full width at half maximum (FWHM) of the Ge films are obtained as a function of heating rate and are shown in Fig. 5.5(a) and (b), respectively. The Raman shift and FWHM of single crystalline Ge are also indicated in each figure for comparison. Figure 5.5(a) shows the Raman shift of Ge film annealed at 220°C and 250°C as a function of heating rate. For the samples annealed at 220°C, the sample annealed with a heating rate of 10°C/min shows a peak position very close to that of a single crystalline Ge. The peak position rises with decreasing heating rate from 10 to 1°C/min, and is almost constant to 0.5°C/min. In the case of 250°C, the peak position slightly shifts higher with decreasing heating rate. The difference in Raman shift is explained in terms of the effect of grain size and stress in crystalline Ge films [1]. Figure 5.5(b) shows the FWHM value of Ge films annealed at 220°C and 250°C as a function of heating rate. The FWHM values decrease with decreasing heating rate from 10 to 0.5°C/min. The smaller FWHM reflects the contribution from larger crystalline size, whereas broader peak implies the existence of a smaller grain [1]. Therefore, the present result implies that a lower heating rate is advantageous in obtaining a larger grain. The samples annealed at 250°C show a smaller FWHM value compared to those annealed at 220°C.

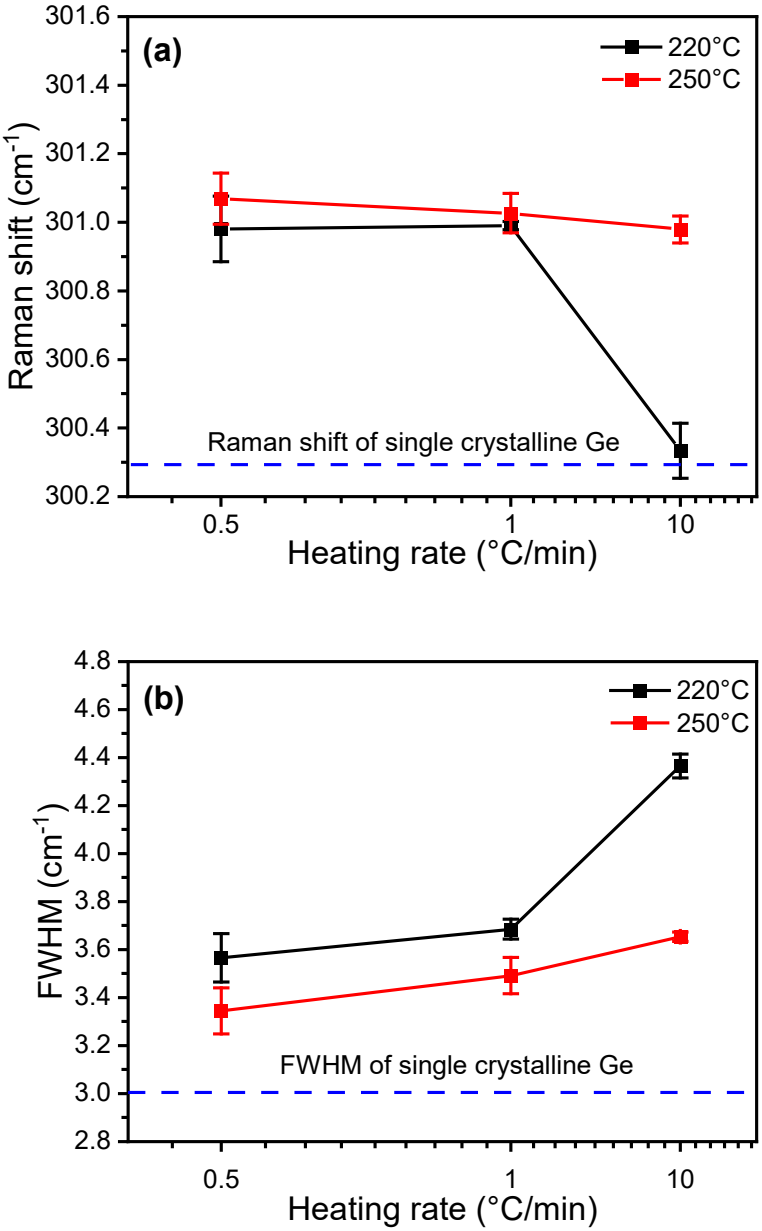

Fig. 5.5. (a) Raman shift and (b) FWHM of Ge films obtained after annealing at 220°C and 250°C as a function of heating rate.

5.3.4 Surface morphology observation by SEM

Figures 5.6 and 5.7 show the SEM micrographs of the samples annealed at 220°C and 250°C with different heating rates. The Au was selectively removed by wet etching process in KI and I_2 solution before observation. The samples annealed at 220°C with heating rates of 0.5 and 1°C/min show very high coverage of 1st layer of crystalline Ge, with a very small number of voids, as shown in Fig. 5.6(a) and (c). The sample annealed with a higher heating rate of 10°C/min, Fig. 5.6(e), has a large amount of second layer and voids in the first layer. These results imply that a lower heating rate is advantageous in improving surface roughness.

Figure 5.6(b), (d) and (f) show the surface morphology of Ge films annealed at 250°C. Although the heating rate dependence is qualitatively the same as the samples annealed at 220°C, the amount of second layer and voids in the first layer have increased by annealing at a higher temperature. It is also found that the films annealed at 220°C have bright areas with a higher Au concentration as shown in Fig.5.8. This implies that an AuGe alloy which has not fully reacted is buried under crystalline Ge. This area could have reacted above 220°C and became a void in the first layer.

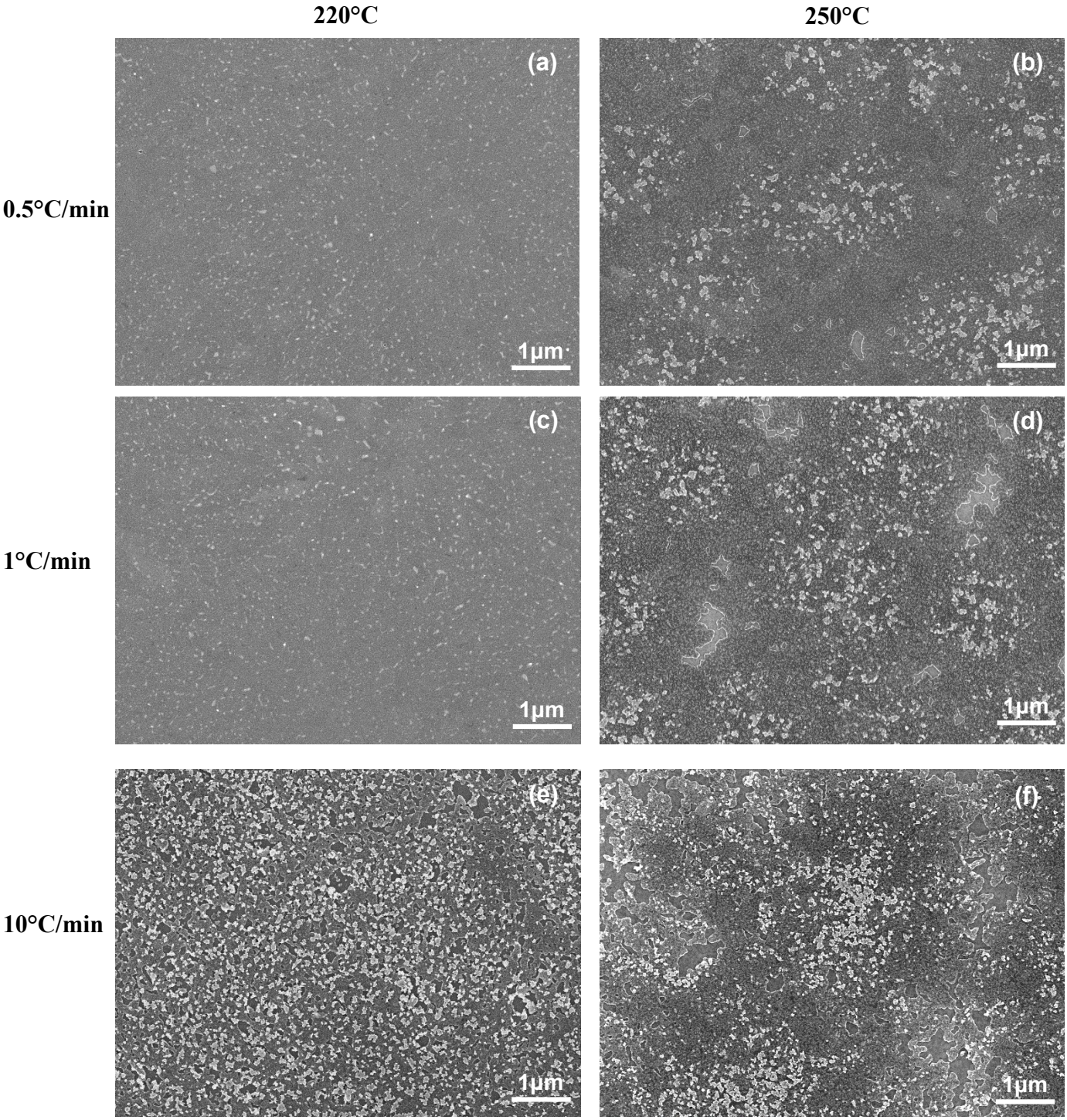

Fig. 5.6. SEM images of Ge films obtained after annealing at 220°C (left column) and 250°C (right column). The heating rates and annealing temperatures are (a) 0.5°C/min:220°C, (b) 0.5°C/min:250°C, (c) 1°C/min:220°C, (d) 1°C/min:250°C, (e) 10°C/min:220°C and (f) 10°C/min:250°C.

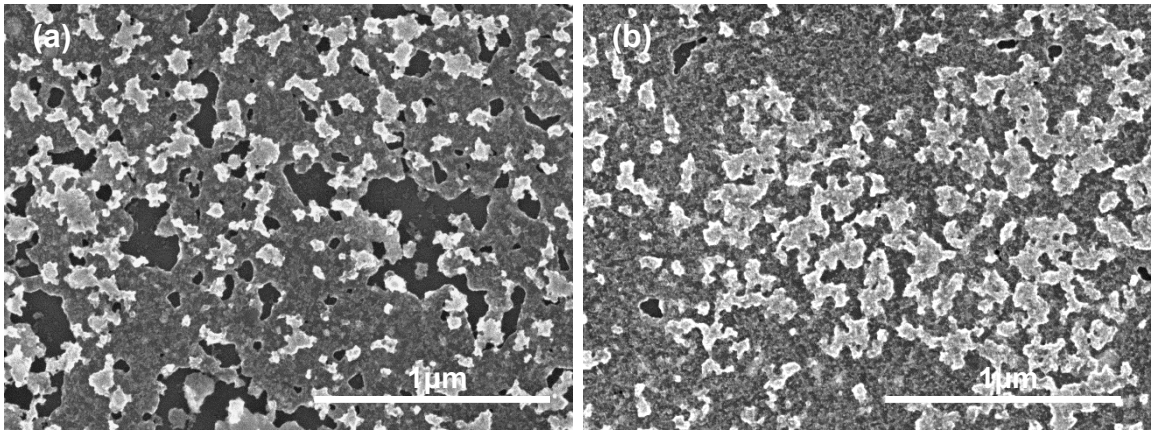

Fig. 5.7. Magnified SEM images of Ge films obtained after annealing at (a) 220°C and (b) 250°C. The heating rate is 10°C/min.

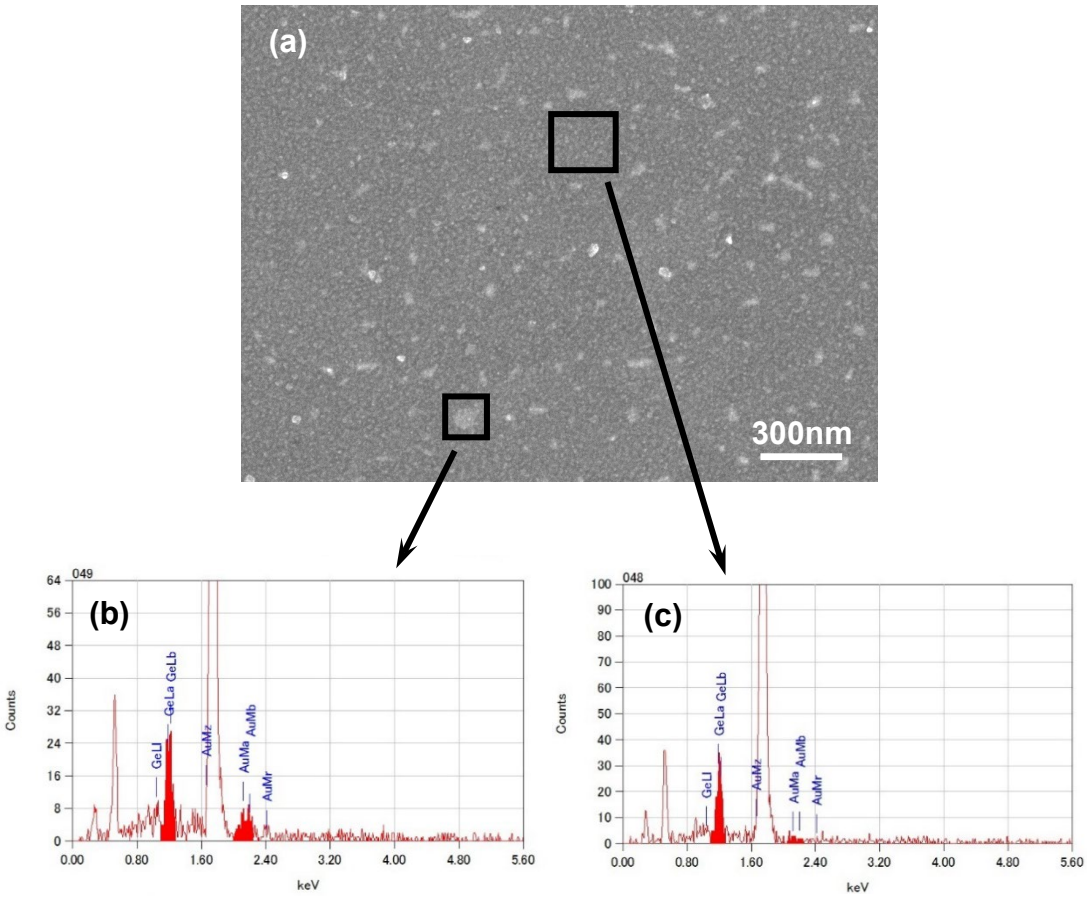

Fig. 5.8. (a) Magnified SEM image of the sample annealed at 220°C with a heating rate of 0.5°C/min. EDS spectra obtained at a (b) bright area and (c) dark area.

The coverages of the 1st and 2nd layers of c-Ge obtained from the SEM images in Fig. 5.6 and magnified images in Fig. 5.7 were analyzed by ImageJ program and are plotted in Fig. 5.9 as a function of heating rate. Figure 5.9(a) shows the coverage of the 1st layer after annealing at 220 and 250°C. The results show that the coverage of the 1st layer increases as the heating rate decreases, where the coverage of c-Ge is as high as ~99% for the sample annealed at 220°C with a heating rate of 0.5°C/min. The coverage of the 2nd layer is also shown in Fig. 5.9(b). It is seen that the 2nd layer increases as a function of heating rate. The samples annealed at 220°C with a heating rate of 0.5°C/min shows a very small amount of 2nd layer. These results suggest that the surface roughness of the crystalline Ge layer could be improved by controlling the heating rate.

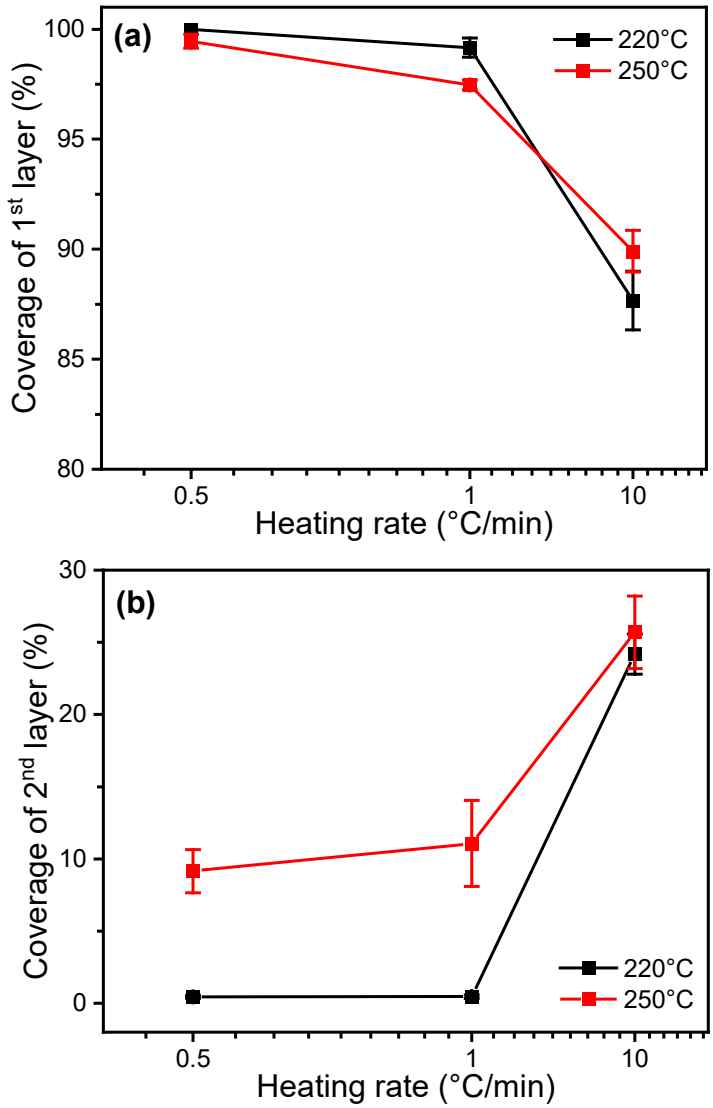

Fig. 5.9. Coverage of (a) first layer and (b) second layer of c-Ge as a function of heating rate.

5.3.5 Crystal orientation and average grain size investigation by EBSD measurement

The crystal orientation was examined by EBSD measurement for these Ge films annealed at 220°C and 250°C. The EBSD mapping images in Fig.5.10 shows the Ge crystal orientation normal to the film plane. The corresponding SEM images of the same area are also shown. It is seen that the crystals are randomly oriented for the 220°C, 10°C/min sample, as shown in Fig. 5.11. This result suggests that the nucleation of crystalline Ge do not occur on the SiO_2 surface, but near the Au/Ge interface [2]. Nevertheless, for other samples, a slightly larger distribution for the (111) and (110) orientation is confirmed. The lower heating rate could have suppressed the Ge concentration near the Au/Ge interface and promoted c-Ge nucleation of a higher atomic-density orientation grain on the SiO_2 surface [2-4].

The average grain size of poly-crystalline Ge was also evaluated from the EBSD data, as shown in Fig. 5.12. The result implies that slow heating rate promote grain growth rather than nucleation and promotes the formation of larger grains. These results are in accordance with the Raman measurement results, where the FWHM of the peaks were smaller for samples with lower heating rates.

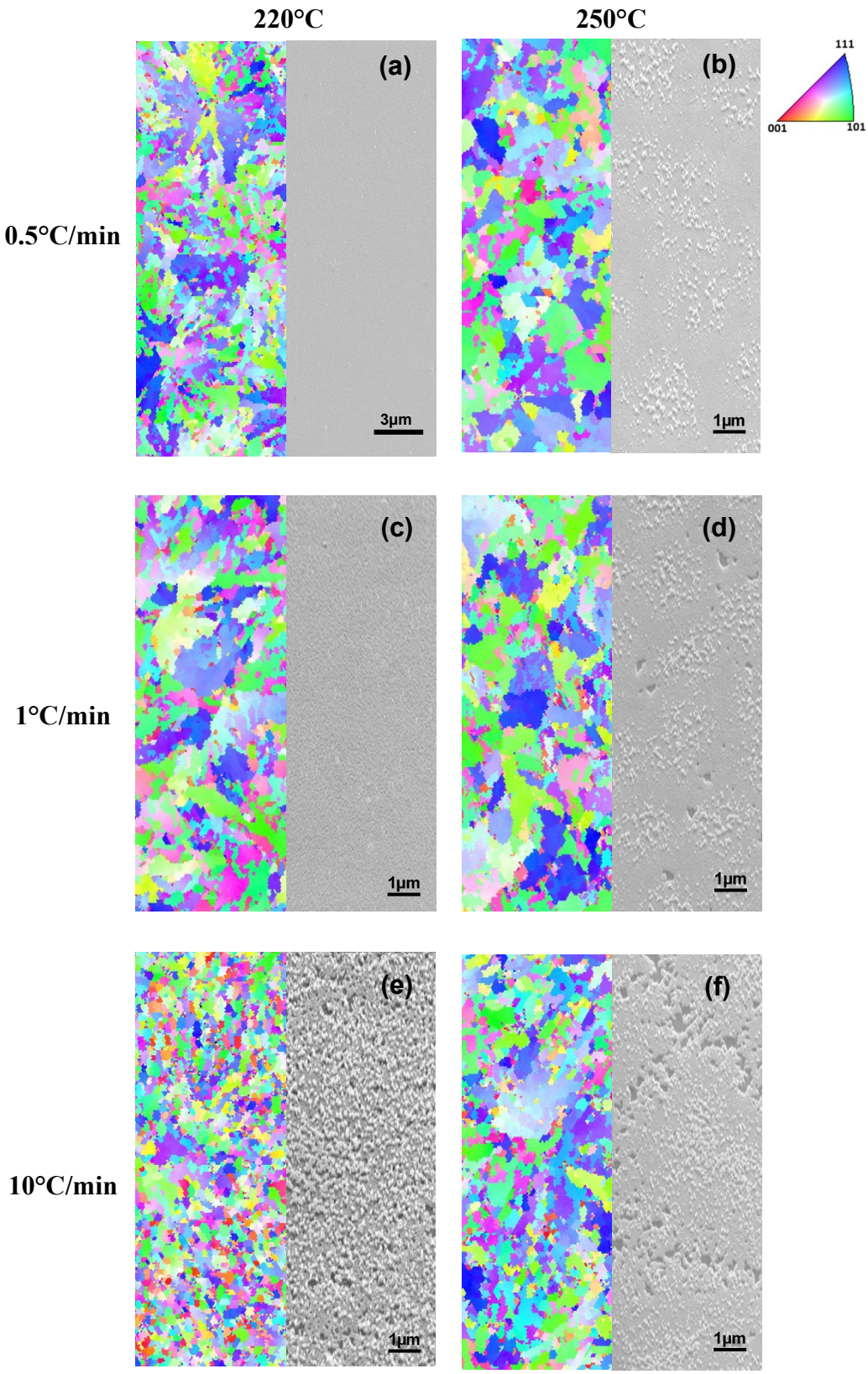

Fig. 5.10. EBSD and SEM images of Ge films obtained after annealing at 220°C (left column) and 250°C (right column). The conditions for heating rates and annealing temperatures are: (a) 0.5°C/min:220°C, (b) 0.5°C/min:250°C, (c) 1°C/min:220°C, (d) 1°C/min:250°C, (e) 10°C/min:220°C and (f) 10°C/min:250°C.

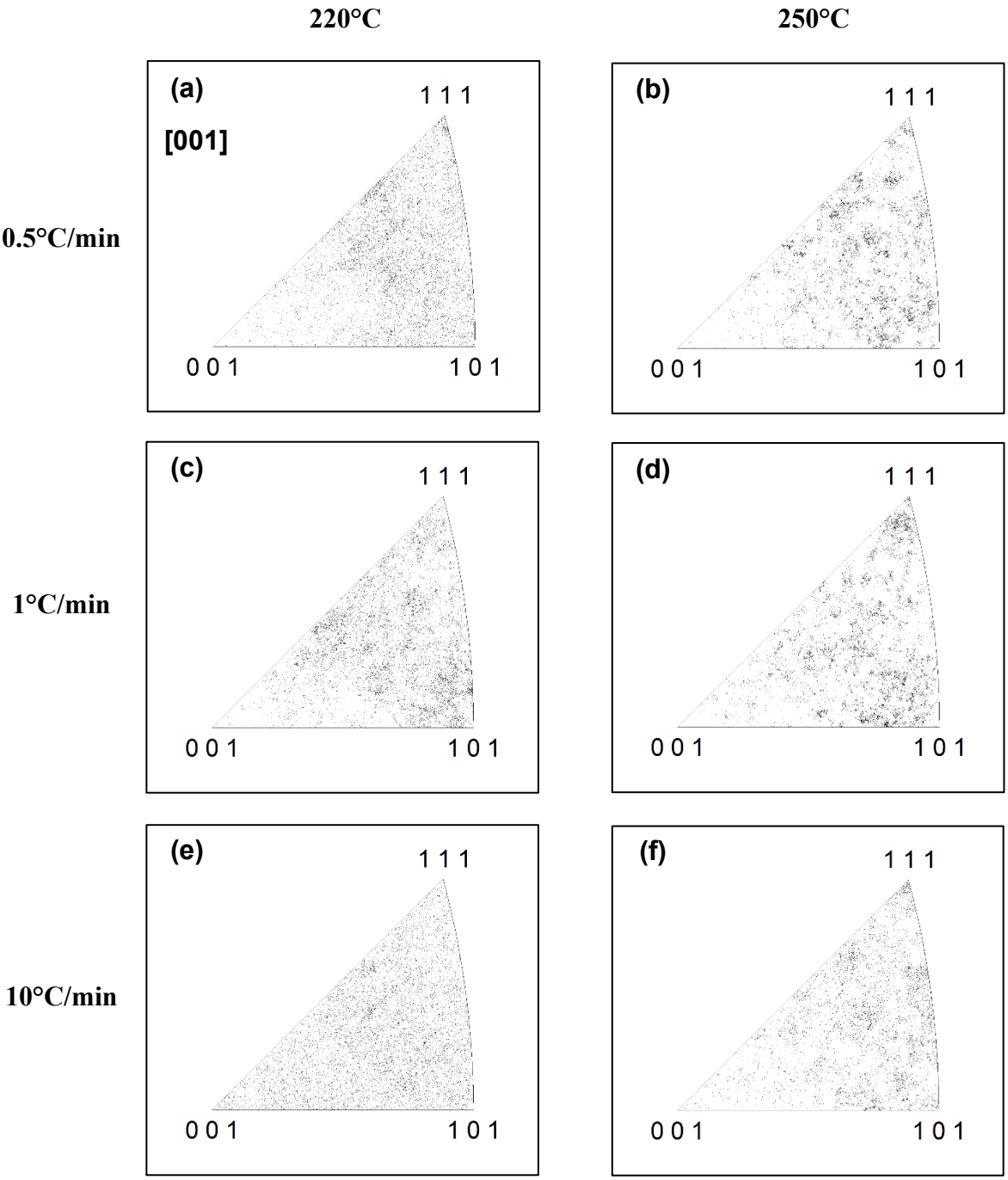

Fig 5.11. Distribution of crystal orientation obtained from the EBSD data. The conditions for heating rates and annealing temperatures are: (a) 0.5°C/min:220°C, (b) 0.5°C/min:250°C, (c) 1°C/min:220°C, (d) 1°C/min:250°C, (e) 10°C/min:220°C and (f) 10°C/min:250°C.

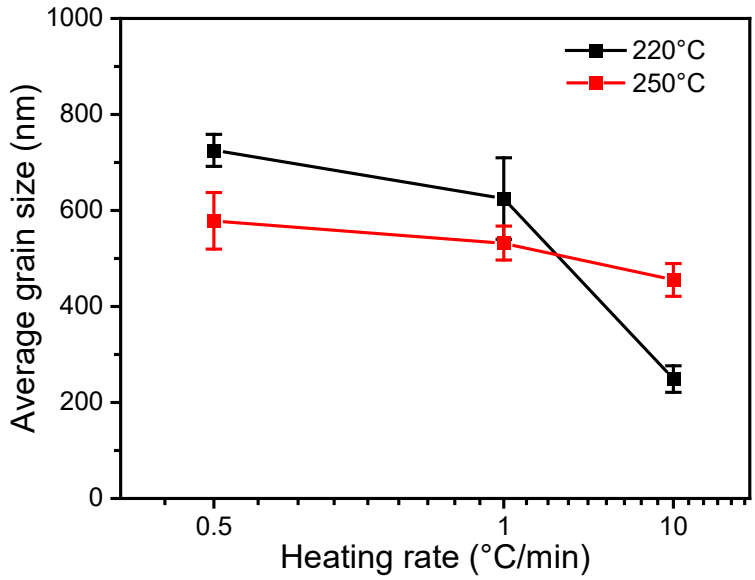

Fig 5.12. Average grain size of Ge films as a function of heating rate.

5.3.6 Electrical property evaluation by Hall effect measurement

To investigate the electrical properties of the poly-Ge thin film, we performed Hall effect measurements in the van der Pauw configuration. Figure 5.13 shows the heating rate dependence, 0.5 to 10°C/min, of the carrier mobility and carrier density of the Ge films. All the samples show a p-type behavior probably because of the defect-induced holes [5, 6]. The dangling bonds in Ge provide shallow acceptor levels and then generate holes at room temperature [7]. The hole density increases as a function of heating rate as shown in Fig. 5.13(a) and takes a minimum value at a heating rate of 0.5°C/min for both 220°C and 250°C annealing. The hole mobility shown in Fig. 5.13(b) tends to increase with decreasing heating rate. The highest hole mobility of as high as ~145 cm^2/Vs is achieved for the Ge film annealed at 220°C by using a heating rate of 0.5°C/min. These results imply that a higher coverage of crystalline Ge and smaller surface roughness for the samples annealed with a lower heating rate, as seen in Fig. 5.9(a), contributed to the higher mobility. Moreover, the larger grain size as shown in Fig. 5.12, could have contributed to the higher hole mobility and smaller hole density [5-9].

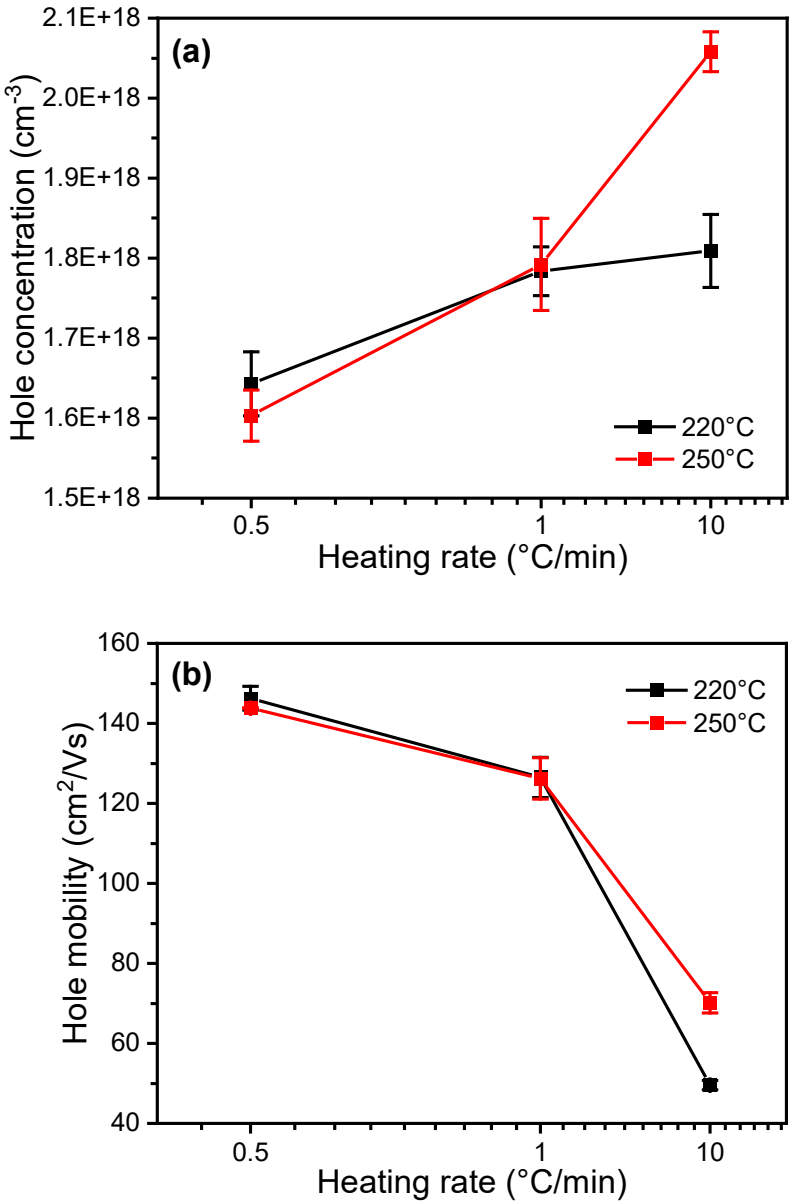

Fig. 5.13. The heating rate dependence of the (a) hole concentration and (b) hole mobility of Ge films obtained after annealing at 220°C and 250°C.

5.3.7 The growth of continuous c-Ge layer with (111) orientation by Au-induced layer exchange

In the previous section, we have found that a very smooth and continuous crystalline Ge thin film can be obtained by adopting a low heating rate. Nevertheless, the crystal orientation was random, and it is desirable to have a (111) orientation to use the film as a buffer layer. According to the result in chapter 3, it is predicted that a thinner Au layer would promote a (111) orientation. In this section, to obtain a smooth and continuous c-Ge layer with a (111) orientation, Au layer as thin as 10 nm is adopted with the initial a-Ge thickness of 18 nm. In order to crystallize the Ge thin film, Au/Ge film was annealed under N_2 ambient with a heating rate of 0.5°C/min at 220°C for 1 hr.

The formation of crystalline Ge has been investigated by XRD measurement. Figure 5.14 shows the XRD profile of Au(10nm)/Ge(18nm) sample after annealing at 220°C with a heating rate of 0.5°C/min. The diffraction peak around 27.3º that corresponds to Ge (111) is clearly observed, which implies that Ge is highly oriented in the (111) direction. The sharp peak at 33° is the forbidden Si (200) diffraction from the substrate. Figure 5.15 shows the SEM micrographs of the sample. It is found that the coverage of the first layer is almost 100% with only a very small number of 2nd layer of crystalline Ge as shown in Fig. 5.15(b).

The crystal orientation was examined by the EBSD experiment. Figure 5.16(a) shows the EBSD mapping image which shows the Ge crystal orientation normal to the film plane. The corresponding SEM image of the same area is also shown. The crystal orientation of this Ge sample is mainly (111), which is in accordance with a large intensity of the Ge (111) diffraction in the XRD profile in Fig. 5.14. This is also confirmed in the distribution of crystal orientation shown in Fig 5.16(b).

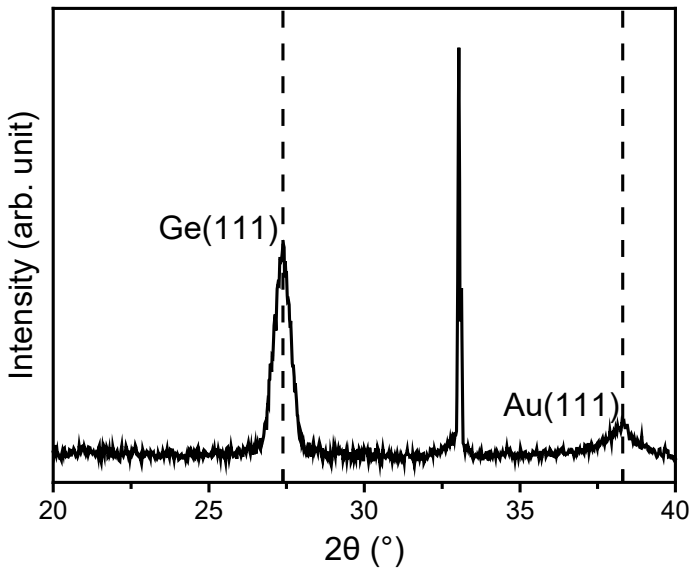

Fig. 5.14. XRD profile of the Au(10nm)/Ge(18nm) sample after annealing at 220°C with a heating rate of 0.5°C/min. The sharp peak at 33° is the forbidden Si (200) diffraction from the substrate.

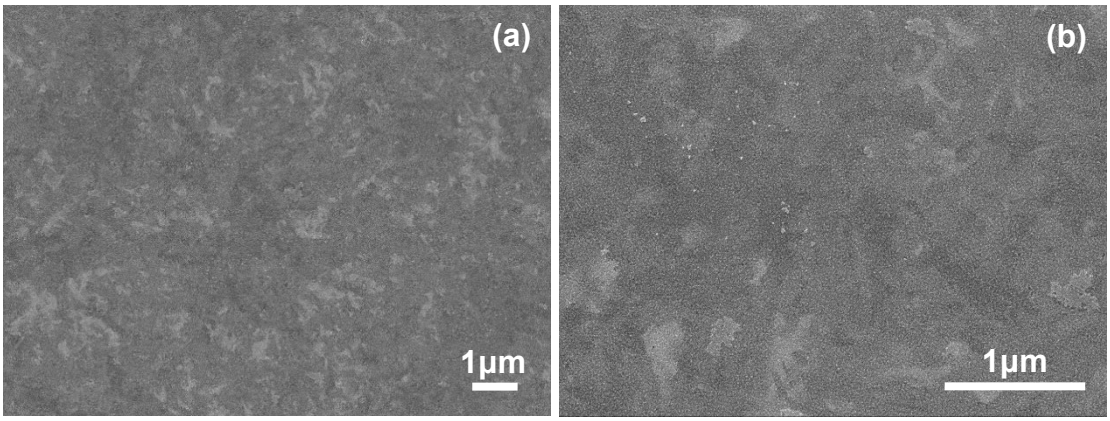

Fig. 5.15. SEM images of the Au(10nm)/Ge(18nm) sample after annealing at 220°C with a heating rate of 0.5°C/min, (a) low and (c) high magnification.

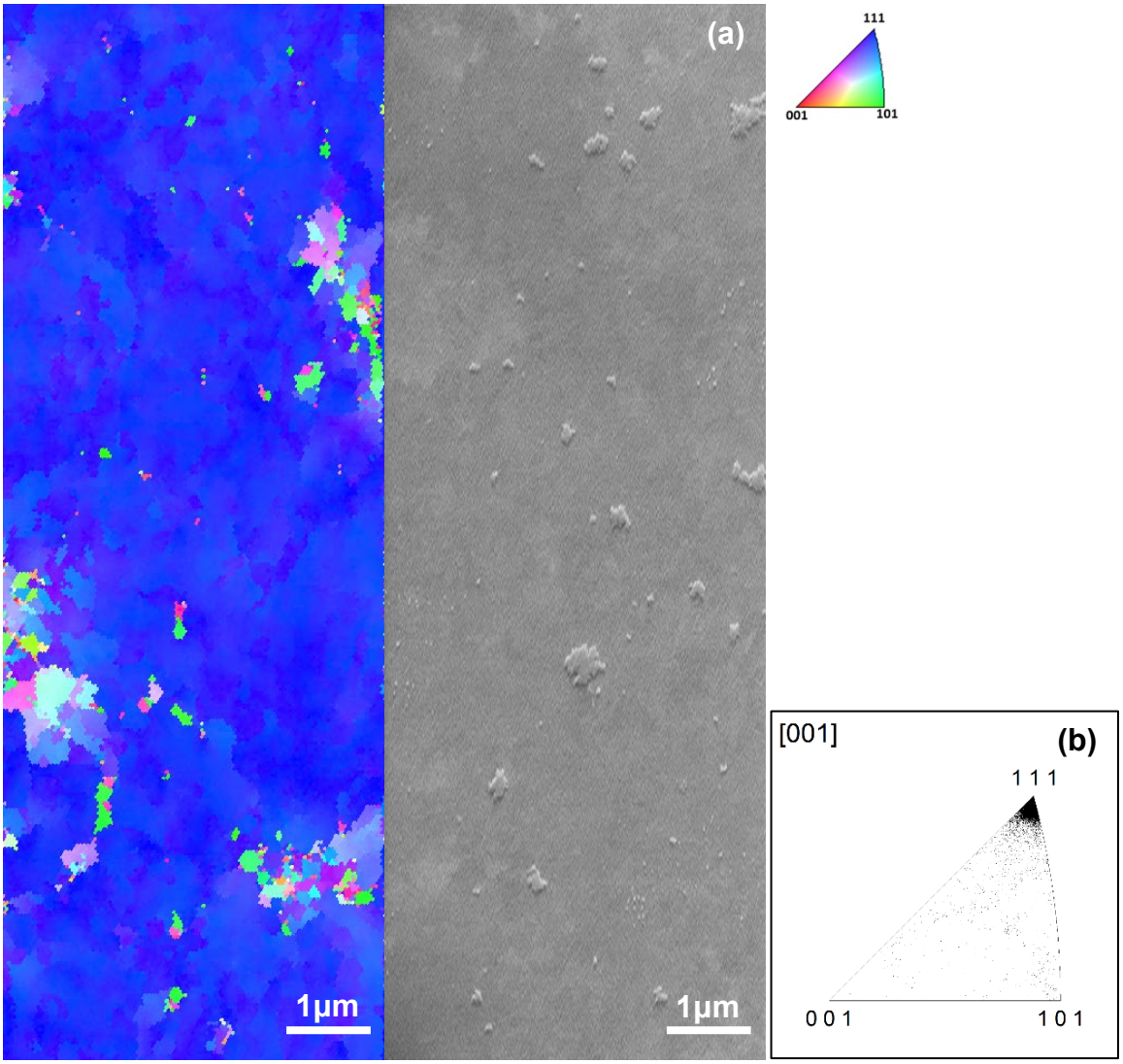

Fig. 5.16. (a) EBSD, SEM image and (b) distribution of crystal orientation of the Au(10nm)/Ge(18nm) sample after annealing at 220°C with a heating rate of 0.5°C/min.

5.3.8 The growth of continuous c-Ge layer growth with (111) orientation by low-temperature annealing

In the previous sections, it is found that a low heating rate is very effective in obtaining a continuous c-Ge layer with a small surface roughness. This implies that annealing at a low temperature for a certain period of time is important. To find the annealing temperature which is important in the crystallization process, a constant temperature annealing at low temperatures has been performed.

In this section, a bilayer with an optimized film thickness of Au(10nm)/Ge(18nm) was annealed at 170°C for a time duration between 0 and 6 hours. The heating rate was 0.5°C/min. Figure 5.17 shows the SEM images of the samples annealed at 170°C for 0, 1 and 6 hours. The image at 0 hours, Fig. 5.17(a), shows that the crystallization reaction has started but is not complete yet. Nevertheless, when the holding time at 170°C is increased to 1 hour, Fig. 5.17(b), it is seen that the first layer of c-Ge is complete. The XRD and EBSD results are shown in Fig. 5.18. The crystallization and (111) orientation is confirmed just as in the previous section. These results suggest that even without the use of an insert layer, a continuous c-Ge layer can be obtained at a much lower temperature with a shorter annealing time.

When the holding time is further increased to 6 hours, Fig. 5.17(c), a small amount of second layer appears on the perfect first layer. This confirms the assumption in the previous section that a higher temperature is necessary to nucleate the second layer which makes it possible to activate only the first layer growth by carefully optimizing the annealing process.

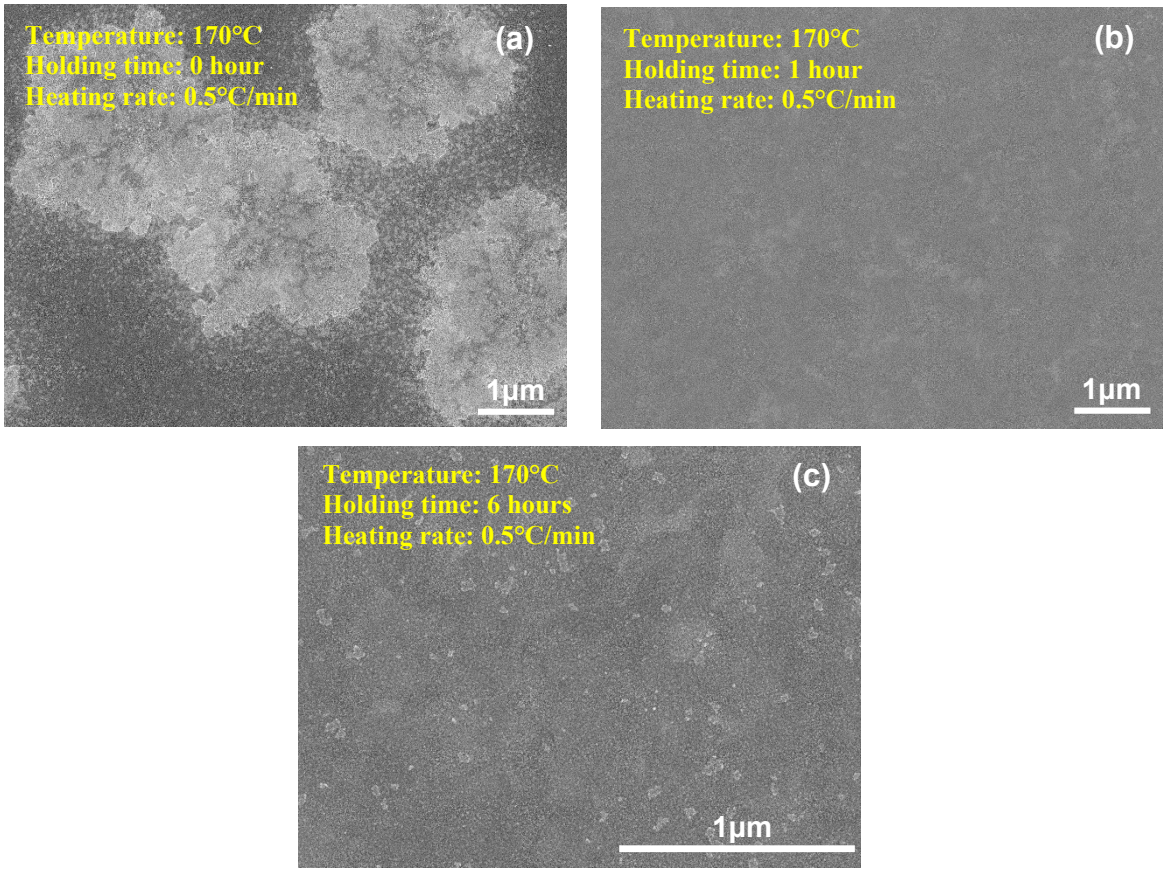

Fig. 5.17. SEM images of the Au(10nm)/Ge(18nm) samples after annealing at 170°C for (a) 0, (b) 1 and (c) 6 hours.

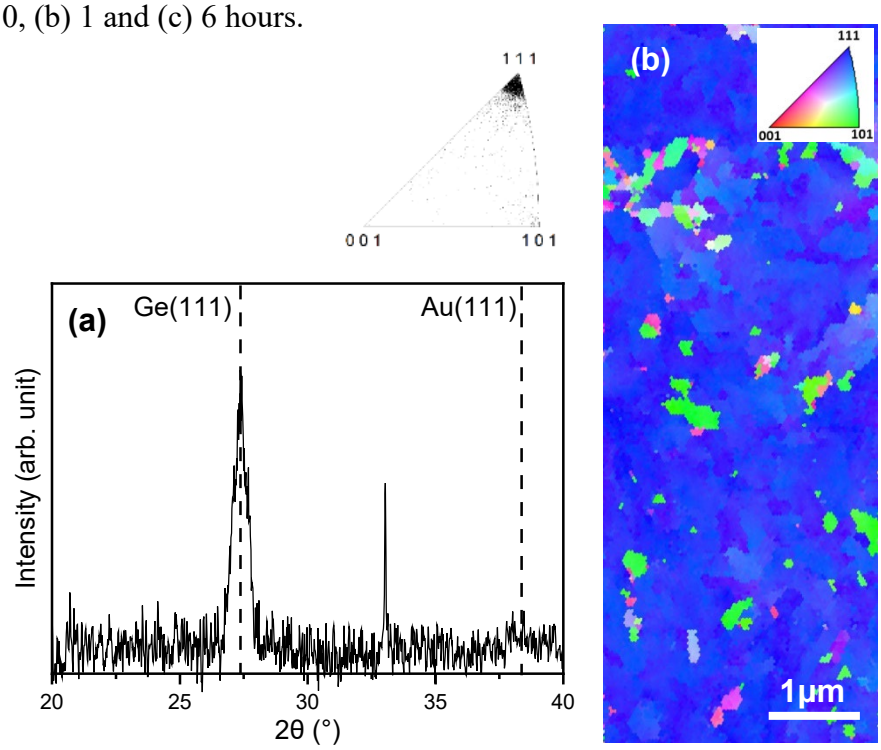

Fig. 5.18. (a) XRD profile and (b) EBSD image of the Au(10nm)/Ge(18nm) sample after annealing at 170°C for 1 hour.

5.4 Conclusion

The formation of a continuous and smooth c-Ge layer using Au-induced layer exchange has been investigated. It is found that the heating rate during the crystallization process is very important and a low heating rate improves film quality. This implies that annealing at a low temperature for a certain period of time is important. A highly (111) oriented c-Ge layer with negligible voids is obtained by annealing a Au(10nm)/Ge(18nm) bilayer at 170°C for 1 hour. These results suggest that even without the use of an insert layer, a continuous c-Ge layer can be obtained at a much lower temperature with a shorter annealing time. The same result is expected for Al/Si and Al/Ge systems where the double layer structure has been observed.

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Chapter 6

Conclusions and future prospects

6.1 Conclusions for each chapter

6.1.1 Chapter 3

In this experiment, we investigated the crystallization behavior of Ge thin films by Au catalysts without an insert layer. By annealing an a-Ge/Au bilayer up to 220°C, it is found that a layer-exchange type crystallization of Ge is possible even without an insert layer. As for the Au thickness dependence, it is found that the best Ge crystallinity is achieved with an initial Au layer as thin as 9 nm. This behavior seems to be brought about by the substrate which promotes heterogeneous nucleation of crystalline Ge. A higher (111) orientation is also realized for thinner Au samples. These findings are encouraging in terms of the smaller consumption of rare metals like Au.

The effect of initial a-Ge layer thickness on the crystallization behavior is also examined. It is found that the initial a-Ge layer thickness affects the morphology of the resulting c-Ge thin films. A double c-Ge layer structure has been confirmed. The bottom c-Ge layer has a thickness close to that of the original Au layer and has a better crystal quality compared to the top c-Ge layer. This morphology resembles that of crystalline semiconductor thin films obtained by annealing Al/Si and Al/Ge systems. It is possible to control the surface coverage of these layers by adjusting the initial Au and a-Ge thicknesses. Nearly 97% of the substrate surface is covered by the bottom c-Ge layer with a small amount of top c-Ge layer by annealing an a-Ge(46nm)/Au(29nm) bilayer at 220°C. The resulting ~30nm thick Ge film shows a hole mobility of as high as ~85 cm^2/Vs reflecting a high coverage.

6.1.2 Chapter 4

In this chapter, the crystallization mechanism without an insert layer has been investigated in detail. The results show that Ge atoms diffuse from the a-Ge layer into the Au layer and nucleation of c-Ge occurs inside the Au layer. Lateral growth of c-Ge proceeds by the Ge supply through the Au layer. This explains why the bottom c-Ge layer has a same thickness as the original Au layer. As the c-Ge layer grows on the substrate, Au is pushed up to the top layer and layer exchange completes.

The top c-Ge layer starts to nucleate at a higher temperature compared to the bottom layer. A poor crystal quality implies a different growth mechanism for the top layer. A small amount of Au diffused into the a-Ge layer could have crystallized Ge without layer exchange.

6.1.3 Chapter 5

The findings in chapters 3 and 4 have been utilized to develop an efficient process to obtain a continuous and smooth c-Ge layer at low temperature. In chapter 4, it is found that the top layer starts to nucleate at a higher temperature compared to the bottom layer. This implies that by annealing at a low temperature for a certain period of time, it might be possible to increase the coverage of the bottom layer while suppressing the nucleation of the top layer. In fact, by annealing an optimized thickness bilayer, a-Ge(46nm)/Au(29nm), at 220°C with a heating rate of 0.5°C/min, the coverage of as high as ~99% for the bottom c-Ge layer with a small amount of top layer has been obtained. This result supports the assumption that it is possible to grow only the first layer by adjusting the bilayer thickness and annealing at a low temperature for a certain period of time which is enough to complete the bottom layer.

Moreover, to obtain a (111) oriented film, a thinner bilayer, a-Ge(18nm)/Au(10nm), has been adopted. By annealing this bilayer at 170°C for 1 hour, a highly (111) oriented c-Ge layer has been obtained with a small amount of top layer.

6.2 Future prospects

A continuous and smooth c-Ge layer can be obtained by Au-induced layer-exchange type crystallization method without an insert layer. The annealing temperature is much lower, and the annealing time is much shorter compared to the process using an insert layer. It is found that three factors are important in obtaining a smooth surface: (1) Optimum ratio of a-Ge and Au thicknesses, (2) annealing at low temperature until the completion of the bottom c-Ge layer, and (3) usage of a thin Au layer. Conditions (1) and (2) are necessary to obtain a complete bottom c-Ge layer without the top layer, and condition (3) is important to obtain a (111) oriented film. These findings will be useful

for the fabrication of high-quality Ge thin films on various inexpensive flexible substrates as a seeding layer for next generation solar cell application.

Nevertheless, the grain size obtained with the present process is still small and there remains a room for improvement. Decreasing the nucleation rate of c-Ge should be important, for example by decreasing the annealing temperature further, but a compromise with the whole annealing time will be necessary.